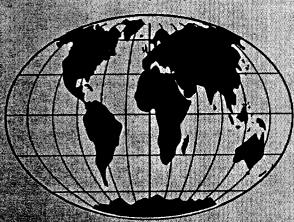
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The Computer Journal

Issue Number 80

Fall 1997

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Founder Art Carlson

Editor/Publisher Dave Baldwin

Previous Publishers Bill D. Kibler Chris McEwen

Technical Consultant Bill D. Kibler

Contributing Editors Ronald W. Anderson Richard Rodman Helmut Jungkunz Tilmann Reh

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Editor's Column

And in this issue...

We have Win95 in the house now. My wife's laptop for work came with it and she's required to use it. The only crashes she's had involve the online connection she uses for work. Otherwise there have been no 'problems' but...

Looking at Win95 on her computer has verified my suspicions about it. The primary purpose of Win95 was to boost lagging sales by Microsoft and the other major PC software and hardware manufacturers. They made enough changes to make sure that your old software wouldn't run as well as their new software. They also made many little changes in the names of things so that finding a function that you used in Win3.1 or DOS sometimes becomes a little challenging.

Another thing is the hardware. Win95 expects certain things from the hardware and can be uncooperative when it doesn't find them. Win95 is 'designed' to be smarter than the average consumer that buys it (and I wouldn't be surprised if it is). It was not intended to cooperate with the minority of us who think we can set things up ourselves. My recommendation is that if you really need Win95, get a new machine that is intended to run it (and save your old machines for your old software). It can minimize the problems you run into.

I'm not against Windows or any other particular software or hardware. The TCJ 'philosophy' is that you use products for what they're good for. I use Win3.1 programs to publish TCJ. No DOS program that I know of will do the page layout that I need. On the other hand, I always make a note of the things that people have done that seem to benefit them more than me. I've paid (a lot) for the software I use and I don't particularly like the idea that I should pay again to do the same thing because someone else needs to sell a new product.

With the exception of Desk-top publishing and graphics, every program I use to make money runs under DOS. Well, actually, SLR's Z80ASM runs under CP/M and it still makes me some money. Obviously, most of the 'big' companies aren't making any money from me at the moment. I'm sure they'll 'get me' eventually. When I just gotta have the latest upgrade, it will be a Win95 version and I'll have to break down and buy a Win95 machine. Then I'll have every thing from my first CP/M machine (a Bigboard 1) to a Pentium here in my office. All I have to do is find a place to put all of them.

Dave Baldwin,

Editor/Publisher

PS: If you find yourself dependent, like I am, on older software, Make Sure You Have Backup copies!! Many companies are out of business and many others won't support their older software.

We lead off with B/P Bios by Hal Bowers and Cam Cotrill. They're still working on it and refining it. Next is my article on the PC serial ports in ASM and C. There have been a lot of requests for working code for the PC serial ports so here are three small terminal programs, two in ASM86 and one in C. This is one of those 'easy' things. One of my customers recently thanked me for doing a custom version for him in only two weeks. I told him it wasn't hard, all it took was ten years preparation.

Allison Parent, a new author for TCJ but an old hand at micros and CP/M, writes about adapting PC hard disk cards to other systems in Cheap Hard Disk Controller. Part 3 of the continuing saga of Simplex III is here also along with Rick Rodman's Real Computing column.

Another new author, André Fachat, presents his High Speed Serial for the 65xx, Add a 16550 to a 6502. He shows what it takes to adapt a chip to a system it wasn't designed for. I'm not sure what the 8250/16550 were designed for, but he has it working with his Commodore C64.

Ron Anderson continues with Small System Support and Bill Kibler with The Computer Corner. Helmut Jungkunz is back with the European Beat this issue with an article about coercing dBase to cooperate with the ZCPR TCAP.

<u>Next Time...</u>

Part two of B/P BIOS is in the next issue along with Ron Anderson's PC serial and parallel port test programs in C. There will be more PC programming articles along with embedded hardware and software in the issues to come.

Don Jhindra, author of The Little Big LAN, is working on some networking articles but I don't know when they will be ready. He's done some fascinating things with LBL. In addition to standard network cards (Ethernet and Arcnet), LBL has built-in support for both serial and parallel ports. I bought a copy but I haven't had time to install it. Since Don also provides programming support, it looks like I should be able to make LBL talk to just about anything.

About The 'Net

by Ted Deppner

New Column

Internet Myths

The Internet: Myth No More

The Internet is the latest storehouse of myths in people's minds. Some myths are heated, (pornography galore!), some are bad (those nasty Internet Police), and the bare truth about the Internet gets little air time. Myths usually talk about what the Internet is, completely ignoring what it isn't. We'll talk about both and give you a more complete view of the Internet as it is, and what it may become.

The Internet is above all else a reflection of society. There is something for everyone online. There are match-cover collectors, TTL chip directories, model railroad fanatics, crocheters and knitters, libraries, state and federal agencies, and so on. (and TCJ, of course) You can find the latest in golf clubs, USR's X2 upgrade, or just the drivers for your sound card. And yes, you can find pornography, political propaganda, and the latest in home built explosives. This is a reflection of society, remember?

Myth #1: Pornography and other stuff. Just like in the physical world around you, you make the choices about where you go and how you spend your time. You make the choices, they aren't forced on you. If you don't like the adult book store, you don't go in. You can just as easily choose the local electronics hut of retired hardware. It's the same on the Internet: you go where your interest are, and stay away from those "other" areas. To each his own.

Myth #2: The Internet Police and Big Brother. Those guys sure do get around. Hah. The Internet is a large collection of cooperating but separate entities—there is no centralized anything. As such, there is no central repository of information, no government affiliation or governmental control, and no police. This doesn't mean you can do anything you want and "get away with it". While there is no central control and record keeping, records are kept.

A record of where you have been, what file you have downloaded, or where you sent email to is kept, but the contents of these items is not. Somewhere deep in your service provider's logs it says "me@here.com" sent an email to "him@there.com", but what the message said is not recorded. There's a log entry that someone at there.com viewed my home page, but who that actually was isn't listed.

Time, date and origination are the extent that is kept. Your name, address, or anything identifying you as "you" are not kept, unless you choose to provide that information. However, armed with time, date, origination, and a court order, your Internet service provider could easily determine who was there at that time.

Myth #3: Etiquette and morals. Moral ineptitude is frowned on by the Internet community. If you send out the latest Make Money Fast file, expect lots of email calling you names. Email 10,000 people your latest sales flier out of the blue and expect your service provider to shut your account off

Illegal activity is always illegal, and stuff you couldn't do in your local communities you can't reasonably expect to

do online either. If you have questions, contact your service provider, they should be more than happy to help you.

Myth #4: The Internet has everything. Well, yes it does, though it may not be exactly what you wanted. Anything that is freely available in the world is online. Works by Shakespeare, Poe, and Doyle, sports scores, stock reports, and so forth. You can find plenty of home built circuit diagrams for all sorts of devices, but you probably won't find the latest schematic for your TV online. You won't find the latest book by Stephen King online, nor up to the minute stock information. You can find reviews of King's latest book, and you can get your stock information delayed by fifteen minutes. Of course, if you want to pay to get King's book you can, likewise you can get your stocks up to the minute if you subscribe to that service.

Myth #5: Buying the Unknown. Everywhere you go in society, you have offers to purchase things: Books, magazines, new computers, the latest Microsoft collection of bugs, and new "must have" widgets. In the real world, you have to pull out the flat wallet, peek through it, and put forth green or plastic. So also goes the Internet. In general, everything online is free. If it is not free, it will tell you so, and make you give your credit card numbers and name before letting you on. You won't just stumble into some pay area and all unknowing start racking up charges. Once again, it's your choice. Good companies will provide a free sample of what they offer, so you can get a taste.

Myth #6: They'll steal my Credit Cards! Recent versions of Internet browsers can encrypt what you're sending, and you can use security programs like PGP (Pretty Good Privacy) for email. Getting your numbers would be a needle in haystack kind of problem in the first place, so add to that encryption of one sort or another, and the fact that there are much easier targets for thieves, and it's not a huge threat. Obviously you shouldn't say "hey everybody here's my credit card", but then you wouldn't do that in the real world either.

The Internet is a vast and wonderful place. It reflects the society of the world around us, and each of us can personally benefit from what the Internet offers. We can each have an effect on what the Internet is, through our participation. There are email discussion groups and USENET news groups with topics that range from iguana care to how to repair TVs. You can even put your own web pages online, detailing to the world how to make the Mr. Spiffy Widget, or simply stating how you made your networked coffee machine. So step forth without fear and newly armed with the truth about these six common Internet myths.

Happy Netting! ======

— Ted Deppner, ted@psyber.com, http://www.psyber.com

Ted takes care of the technical stuff at Psyberware where the TCJ Web pages are located.

Letters and News All Readers MINI Articles

READER to READER

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From: Christopher Burian cburian@ll.mit.edu

Subject: 8051 Startup code in TCJ #78

Thanks for this great article. It's the best, maybe only, article I've seen yet that implements working interrupt-driven serial and circular queues.

I'm astounded by all the sample code out there, even sophisticated-looking monitors, that use queueless polling to send and receive. It's either that or generic pascal-like junk found in next-to-useless textbooks.

Luckily, I had a college class on 8088 assy programming which included a unit on circular queues, interrupts, programming the 8250 uart, etc., but most people don't get that kind of class. I guess it's considered unorthodox and out of the mainstream to actually teach students how to write real programs that run on genuine CPUs. Entirely too much programming at my U. was taught in virtual languages which were compiled and simulated on virtual computers existing only in the perverse imaginations of CS professors. So I think lots of people are going to find your 8051 introductory article really useful, as I have.

Despite my previous exposure to queues, your sample program is a great help to me in simplifying my own code.

I wish you'd had a little more time/ space to delve into the problem you discovered wrt interrupt code on NMOS vs. CMOS chips, and perhaps given an example of code ordering which you found not to work, just in case someone decided to make modifications to your code. Unlike the hcll's protective feature (write within the first 64 clocks only) the problem you've discovered sounds more like a bug than a feature.

On my current project, I'm again reinventing the wheel, making a monitor/hex-downloader, because just like lots of other guys, I think I can do it a tiny bit better. One of the gimmicks I want to include and haven't seen anywhere is intelligent handling of BREAKs sent from the host. Another is use of handshaking when queues fill up, to handle delays when programming FLASH during a hexfile download, for instance.

I have a couple questions about your QUE_SND routine. Why isn't a CLR C required before the SUBB? And why use SUBB instead of CJNE?

Thanks, and keep up the good work. Eagerly waiting for #79,

Chris Burian

I'm glad you liked the 8051 article. TCJ #77 had an article with similar code for the Z80-SIO and this issue has my article on the PC serial ports.

Inever did find what the original problem was. I'm sure it's a 'bug' of some sort. The Intel 8051 experts couldn't figure it out, may not have been interested. The original program I started out with was SKELETON.ASM from the Phillips BBS and it didn't work on the CMOS 80C31. I don't know whether it worked on the NMOS version. I got a copy of one of the standard, polling monitors from a friend and it worked on all versions of the chips. That verified to me that the chips were working and that I just had to do something different with my program. I went back to the books to see what might be dependent on the sequence and this program is where I ended up.

About the QUE_SND routine, the 'CLR C' probably should have been in there. After looking at the program, it's probably just an accident that it works without it. 'CJNE' tests for the wrong thing in this case (NE). I needed to know if it was equal to 10h. A TX_CNT of 0 means that all bytes have been sent. I to 10h means that there are bytes to be sent in the fifo and 10h is the max the fifo can hold.

Dave Baldwin, Editor

From: "Jeffrey A. Weiner" <j_weiner@juno.com>

Subject: XT's and kindred folk

Kudos on Issue No. 79! Well worth the boost we all gave you.

I also wanted to note that its a good thing that TCJ is covering XT-class machines. Case in point: I rescued 3 ALR Barrister XT system units from the dumpster of the building I work in. ALR had scant info on the motherboard switches, and nothing on the unique combination controller card that was in the beasties; connections for 2 pairs of floppy drives, serial and parallel ports, clock/calendar, and a mysterious 50pin header marked "HIGH DENSITY DRIVES". I'm hopeful that a someone who reads/ writes for TCJ will e-mail me some info on this card so's I can take advantage of its features.

And those kindred spirits? Well, one thing I'd like to see is some articles about doing something useful and/or different with a DEC Rainbow. I have a few (!) of them on the premises, and

since the International Rainbow Users Group has hit the bit-bucket, it would be nice to see some guidance from some more technically-adept Rainbow afficianados.

Keep 'em flying...

Jeff Weiner Chicago, IL

From: Ron Anderson

<rwilande@concentric.net>
Subject: Hard Drives

Dave.

Last July my Conner 830 Mbyte hard drive crashed. It was eleven months old. Knowing that it would take a while to get a warranty repair, and having a use for that drive in another system, I bought a new Western Digital 1070 Mbyte drive as a replacement.

Conner had just been bought by Seagate, and partly due to transposition of two digits in the Return Authorization number (my error, not theirs), it took about six weeks to get the replacement drive back. Either they sent a new drive or they replaced the tag on it, because the new one said Seagate on it.

Shortly after that, I went to "defrag" the new WD drive and an error message appeared saying that parts of the disk were not accessible. I ran "scandisk" on the drive and it found about 1 megabyte of bad sectors all in the last 150 or so tracks of the 2488 on the drive. I decided to watch the drive carefully and to call WD if more bad sectors were mapped out later. Last month the drive failed a defrag session again and I found that another 400K of sectors had gone bad.

I called WD and they asked me to download a diagnostic from their web site and run it on the drive, and call back to report the result. The next day I phoned them and they said the drive was bad enough so they would replace it under warranty. With my credit card number as collateral, they sent me a new drive and I transferred a large number of files after reinstalling DOS and Windows 3.1 on the new drive. I ran scandisk again and before I had all the software installed, I noted some bad sectors had to be mapped out, again all at the very end of the drive.

About at that time, my replacement Seagate drive quit completely. It

sounded like the head servo had gone crazy, and couldn't read data from the drive. I called Seagate and after ten minutes of tone button pushing on their "automated service line" the computer gave up and informed me that there was a problem and transferred me to a real live person, who was most helpful, agreed that the drive was under warranty, and gave me a return authorization number. This time I was careful to see that I got it right, and I have sent both drives back to their respective manufacturers.

The next day, I was talking to a friend who is experiencing the same difficulties with a Western Digital drive. He reported that about 6 megabytes of sectors had been mapped out, and that the bad list continues to grow. He has run the WD diagnostic and was planning to call for authorization to return the drive last time I talked to him.

Could it be that the manufacturers in their race to cram the most data in the least hardware have pushed the technology beyond the limit of reliability? I've used Western Digital drives for years, and in fact have a couple still running that had never had a problem (an old 100 Mbyte drive and a 170 Mbyte).

I've ordered a "refurbished" 650 Mbyte drive to have around as a spare. Maybe this one was before the technology got pushed into the area of unreliability. We'll see what happens with the Seagate.

I must add that I was treated very courteously by both Seagate and Western Digital's service people. The wait was minimal (a few minutes) in both cases.

Ron Anderson

From: Ken Deboy

Dear Bill,

I figure that if I'm going to criticize Windows95 and Microsoft, I should explain some of the problems I've had with Win95 and in dealing with Microsoft, so here goes:

1. The pamphlet (no way it could be called a "manual") doesn't explain how to do anything. For example, I had to call a 3rd-party software vendor to find out how to over-write the MBR so I could install System Commander

(Win95 doesn't normally allow this to be done). Microsoft was no help because they won't provide tech support to someone who obtains Win95 preinstalled on their computer. (I could really get into what I think about a software company that won't support their own damn OS, but I won't.)

- 2. It sometimes locks up on me, with no way to recover except turning off the computer. Of course, there is a dire warning in the pamphlet to never do this, but what else is there to do when even <CTRL-ALT-DEL> doesn't work? Never had this problem under Win3.1 (or Linux or OS/2). This isn't a "rare" occurrence, either...at least 3 times a week, sometimes even twice in one day.
- 3. It won't let me delete DLLs from .../WINDOWS/SYSTEM even if they're not write-protected. It also won't let install programs over-write them if one tries to install a DLL that is already there. I have to drop back to DOS to delete the file, which is fine, since I know how to do it (no thanks to Microsoft), but what about the poor soul who has a Win95 box as their first computer?

There are other minor frustrations with Win95, but these are the major problems I have with it. Sorry for the rant, but I don't feel right criticizing a product without explaining why I feel the way I do. I hope Caldera wins their lawsuit against Microsoft, but I'm not betting on it. I feel the only way to make sure MS doesn't become a monopoly is to make sure that other OS's are economically viable. I have OS/2 on one computer, and soon I'll have it on both my computers. When I need a program, I try to find a version that will run under OS/2 or Linux. If I need a program that is only available under Win95, I always make sure to write to the software company and tell them I'd be interested in purchasing a version of the program to run under OS/2 or Linux. Maybe if enough people did that, MS would lose the strangle-hold they have on the PC software industry. Well, at least I can dream...

With best wishes, Ken Deboy From: Steve Johnson

Dave:

Enclosed is my early renewal check for

TCJ.

Detailed comments about the magazine should wait for a future message, but you should know that I always read the magazine with a day or two of arrival and I continue to use the complete set in my study. I like the practical, problem solving approach authors take and the mix of diverse hardware, operating systems and languages covered. Even when I'm unlikely to work with a particular combination of hardware and software, I enjoy the articles and learn of practical value.

Subjects of particular interest to me are small scale networking and operating systems including Linux and Forth. CP/ M remains of interest and I follow 'comp.os.cpm' closely. Like many other readers, I run MYZ80 instead of nursing my (diminished) accumulation of aging Osbornes and their many accessories. During my last binge of old equipment accumulation, I picked up a dual set of Siemens 8 inch drives which interface to an Osborne Executive with quad density internal drives and dual external hard disks. It pains me to admit it, but the Osbornes are less robust than the Kaypros.

Rick Rodman is one of my favorite TCJ contributors. My at-home computing network is much less elaborate that the Kettlepond Computing facility, which serves as inspiration. I believe my next networking step will be to extend the thinnet from the second floor to my basement workshop & home brewery (well I do have other interests besides computers). That will be a natural time to get involved with home monitoring and control.

Enough comment, time to write a check.

Signed: Steve Johnson

From: Rick Bromagen

To: Dave Baldwin

Hi Dave!

I just received the last issue of my subscription to TCJ (#79), and that re-

minded me there was something I have been intending to do for several months now. It's time to renew my subscription! Let's have 2 more years please.

I had been trying to figure out how to add an IDE interface to my Z80 CP/M system for several years. Then TCJ published the articles from Tilmann Reh. That was great work! We all owe people like Tilmann a big thank you. Those that have the time, knowledge, and are willing to share their efforts with everyone else have my respect.

I assume there are at least a few who have built the GIDE interface by now, and have done some tinkering with BIOS driver software. Of course we all seem to have different systems and BIOS's, so sharing source code is not simple. I am planning to put a GIDE on my Eagle II mother board. It already has a SASI (early SCSI interface) drive, but I like the challenge of putting a much faster and bigger drive on this system.

That reminds me, I would like to hear in TCJ about different ways to add large hard drives to CP/M. By that I mean how to have a 40 or 80 megabyte CP/M drive "partitioned", and how the BIOS tables describing it look. I think Ampro and several other had done this. Is there a public domain description or code sample for this?

That TCJ centerfold about the P112 board looks very interesting to me. How can I get one of these? When will TCJ offer a group buy? I am busy thinking up several projects I could "embed" this and a drive into. How about an embedded household controller with floppy (ala Circuit Cellar Ink HCS II), or a portable CP/M system? I remember David McGlone of the Z-Letter once mentioned that there was a computer built in a small, flat portable case, with maybe an LCD screen. Maybe I will try pulling the Z80, and putting the P112 board with a 3.5" drive. How about a 2.5" hard drive as well? Of course, battery power will need some thought. There are a lot of high power replacement batteries for laptops available now that could be small and light weight enough. It would be fun on my next long airplane trip, to pull out a CP/M laptop, play some games, or even do some writing.

DisConnect

Dogbone McGillicutty groaned when he heard the 'snap' that told him his network fiber had popped out of the wall. He was just trying to move his workstation a little bit to make some room. He started imagining the parade of people he'd be seeing soon. First would come the Nettertons network security people to see what had happened to 'their' connection. Of course, none of them could repair the break, but they could cite you for 'Illegal Disconnect', section blah-blah-blah of the Network Code. They would tell you to get it repaired right away. If they were in a good mood, they'd call repair for you since, of course, you couldn't because you just broke your network connection.

The last time he had called repair was from a friends terminal. First, they asked why he was calling since the system was obviously operating since he was able to call them. Then they wanted to know why he was using someone else's station and did he have permission to do so. After identifying himself, his employer, and his station and waiting for them to verify that he wasn't home using his station, they finally agreed to come repair it although they warned him that he would be charged double if it was a UIP (User Induced Problem).

After (or maybe even before) the repair droids showed up would come the HW2020 (Home&Work) people to find out why he wasn't using their systemware for his each and every need. And somewhere in one of those groups would be a Copper-Checker to make sure he wasn't one of those that had found out how to blackbox the old copper network and avoid his responsibilities (and payments). And after all of those people were done, he'd have to go through a reconnect session and verify his ID and his accounts and all of his passwords which would take a half a day. Can't have any illegals on the Net.

Banked/Portable I/O System (B/P Bios) Pt I

by Harold F. Bower and Cameron W. Cotrill

Special Feature
Z80/180 Systems
Advanced BIOS

For the past several years we have attempted to address some of what we consider to be fundamental problems in the 8-bit Z80/Z180/HD64180 system software arena. Our first effort, ZSDOS, was directed toward what we believed to be architectural weaknesses in CP/M and its clones in the late 1980s. Such weaknesses included; inefficient code, inconsistent implementations of some DOS functions, numerous different and incompatible file Date/Time Stamping methods, and just plain errors (remember Function 37?). Now in the 1990s, even more effort is needed to correct the proliferation of systems designed on faulty (or at least weak) architectures, and to provide a logical and consistent path to increase the functionality of our systems.

To understand our concerns in this area, let us review the way in which CP/M 2.2, as modified by the Z-System, uses available memory. For standard CP/M and compatible systems, the only absolute memory addresses are contained in the Base Page which is the range of 0 to 100H. All addresses above this point are variable (within certain limits). User programs are normally run from the Transient Program Area (TPA) which is the space from the top of the Base Page (100H) to the base of the Basic Disk Operating System (BDOS). Figure 1 depicts assigned areas pictorially along with some common elements assigned to each memory area.

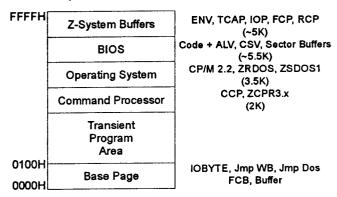


Figure 1. Typical Z-System Memory Map

The sizes depicted for the Z-System buffers is typical of many, and allows a certain functionality. It is sometimes necessary to delete some capabilities to add others, since every addition in this area pushes the other components lower, decreasing available TPA space. Likewise, any new features or more elaborate routines in the Bios decreases available TPA.

There have been some attempts at ameliorating these difficulties, but none have directly addressed the entire problem. One system in relatively widespread use is NZCOM. It allows a fairly easy method of changing systems "on the fly". The main drawback, however, is that to obtain large TPA, system features must be sacrificed by deleting or downsizing the resident Z-System segments (FCP,IOP,RCP,NDR,TCAP). To us, this method is only viable in systems which do not have extended memory capabilities. With the ever-increasing use of systems based on the Hitachi 64180 and Zilog Z180, other solutions are more attractive and offer a larger TPA without sacrificing system capabilities.

The final major factor contributing to shrinkage of TPA is the increasing commonality of large hard disk drives. Disk space is managed by a bit-mapped buffer (ALV) where each bit represents an allocation block of storage space. Typical allocation units are 2k for floppy diskettes and 4k for Hard Disk Partitions. Assuming 4k allocation blocks, a 20 MB drive needs approximately 20000/4 = 5000 bits or 625 bytes. With 80 to 100 MB drives being common these days (one B/P user reported that the smallest drive he could obtain was 850 MB!) you should see that several kilobytes are now required, further reducing available TPA space.

The first requirement to place us on the road to more powerful systems is to overcome the 64k memory limit imposed on direct access by the Z80 family of processors in a consistent and logical manner. Such a technique, generically called memory banking, means that we can access more than 64k of memory for something more than simply a RAM disk.

One of the first attempts to tackle the 64k memory barrier was Digital Research with CP/M Plus (aka CP/M3). While it banked both portions of the BIOS as well as the Basic Disk Operating System (BDOS) and included some useful additions to the BIOS, it was relatively incompatible with CP/M 2.2 in many key features. In addition, CP/M Plus made no provision for banking application code. The adoption of a CP/M 2.2 standard for the Z-System has served to widen the compatibility gap even further on the majority of our systems.

There are some internal inconsistencies in the CP/M 3 architecture as well which were never fully resolved. A prime case in point is the function to return Disk Free Space

(Function 46). The specification states that three bytes are returned reflecting the number of available 128-byte records on a disk. This equates to 2^24 * 128 or 16,777,216 * 128 = 2,097,152 kB. While we know of no one who has actually installed a single disk partition of more than 2 Gigabytes on a Z-System, it would create problems since CP/M Plus can handle disks up to eight times this size, but not correctly report free space. Simply returning free space in terms of 128-byte records is inconsistent as well since disk space is allocated in blocks which have a minimum size of 1k, with 2k and 4k commonly used. This is only one example of several, and we do not consider it a viable system for future Z-System growth; although it is still being actively installed.

Several manufacturers have attempted to bank portions of operating system software over the years, yet either locked the software into their hardware as Epson did with the QX-10, or made such changes as to limit portability of common tools as in the XLM-180. This latter system, while it used the Hitachi 64180 processor with its memory mapping capabilities, required system tailoring of much of the common Z-System software base.

The release of MicroMint's SB-180 in the early 1980s marked a decision point in Z-System development. First, it retained all standard ZCPR3 definitions, it used a CP/M 2.2 compatible BDOS, and it forced programmers to think more of portability and compatibility in system software. This was a major thrust in the development of XBIOS which placed the greatest possible amount of BIOS code in alternate memory locations outside of the primary 64k address space. Furthermore, capabilities to bank additional features (Resident System eXtensions, or RSXs) were widely supported with DateStamper, DosDisk and others requiring no sacrifice in TPA to execute. Since its last upgrade, however, several severe problems have come to light, among them are the inability to properly handle hard disk sizes greater than 32MB and sluggish performance due to banking of Console routines.

We considered this history and wanted to develop a system which included as much machine independence as possible. Not only should newer systems with the 64180/

Z180 processor be included, but S100 systems with banked memory, addon boards such as Terry Hazen's MDISK for the Ampro Little Board, and homebrew systems as well. The goal here was as much selfish desire as anything else. By developing a single common architecture, only one tool for a given purpose would be needed across a variety of machines. As an example, Hal has several YASBECs, two SB-180s (one modified with static memory), an SB180FX, an Ampro Little Board, a couple of mongrel S-100 systems, and recently acquired a P112. Each system had its own Formatter, Configuration utility, Clock type, native disk formats, etc. To us, this seems out of place now, particularly with the scarcity of systems programmers in the Z-Community. It made more sense to develop a common software architecture so that more programming resources could be devoted to applications type efforts.

Another goal of the effort was to retain the maximum compatibility with existing Z-System software for the same reasons cited above. Customizing a huge number of common utilities as was done in the XLM-180, seemed to be the wrong approach. We therefore decided to retain the greatest possible commonality with CP/M 2.2 (actually our ZSDOS), and use existing Z-System segments to their greatest potential without sacrificing performance. As those of you who tracked our efforts as we developed ZSDOS know, we do not like slow systems or large code sizes (TCJ issues 37 and 38). We also decided that our architecture had to be capable of outrageous expansion and extension capabilities without invalidating previous software efforts. Further, we wanted to create a general purpose banked memory interface that allows applications programs as well as the operating system to access alternate banks of memory. The final results are the Banked & Portable (B/P) Bios.

B/P Bios attacks the memory problem in a manner which is easily adaptable to different hardware. All HD64180/Z180-based systems bank memory in 4k slices, and many S100 and addon systems bank in 16 or 32k increments. We therefore decided on an architecture which retains common memory in the upper 32k of address space (8000-FFFFH), and switches the lower 32k (0-7FFFH) among any available banks of RAM. Figure 2 displays this architecture pictorially.

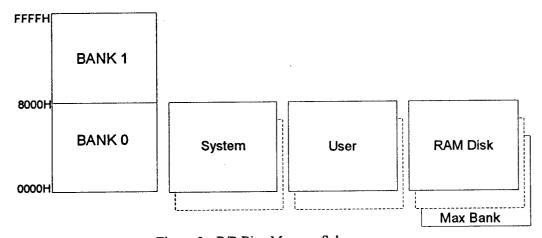


Figure 2. B/P Bios Memory Scheme

BNK1 is ALWAYS present in the address space and is referred to as the Common Bank. It contains all Z-System buffers, Common portions of the Bios, BDOS and the Command Processor as well as the upper portion of TPA. Part of the Bios which makes B/P unique is the structure which allows controlled access to other banks in the lower 32k.

At least one 32k bank is required in a minimal banked B/P system. The system bank, as a minimum, holds portions Bios and a copy of the Command Processor which speeds Warm Boots by simply copying the banked code to the Common bank and executing the warm entry. Figure 3 depicts memory use in a maximally-configured banked system. In such configurations the System bank holds banked portions of, the ZSDos2 operating System, banked Command Processor, BIOS, and Hard Disk allocation bit maps.

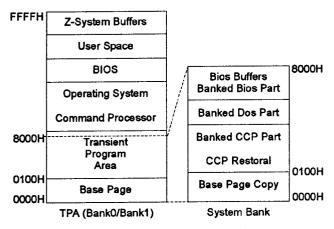


Figure 3. Fully-banked Memory Map

The B/P Bios began with one of Cam's superb architectures. He started with the standard CP/M 2.2 Jump Table, added in those from CP/M Plus with changes to correct some of the inconsistencies, then added in a new series to permit logical and easy access to new routines. The code, in assembly source form, was divided into logically functioning elements, with the greatest possible amount placed into machine independent modules. As an example, the Disk deblocker and IOBYTE decoder functions are machine independent and need no change between systems, while the actual disk and character device drivers require custom tailoring for each type of computer. Standard interfaces, in terms of register usage and value limits, result in common software requirements across vastly different hardware systems.

Each software module of the Bios includes relocation directives to the assembler telling it whether the code is to go into the main memory, or into another bank of memory. If a non-banked system is assembled, all code is placed into the main 64k area, while banked systems use the main 64k area for common code and data as well as banked code and data areas. All tools (formatter, configuration utility, etc) automatically accommodate both types of Bios without any intervention. The choice of whether to bank each section of code or not was painstakingly examined for performance and size penalties. Many of our design choices may be debated, but B/P is here and it works!

By itself, fixing the Bios is not a complete answer to our current Z-System dilemma, but it is a prerequisite. We also considered it essential to bank the Disk Operating System. Starting with ZSDOS, Hal used the new BIOS banking functions to bank significant portions of the BDOS. At every juncture, size and speed were traded off to keep the system small and fast. We corrected the flaw in the CP/M Plus Disk Size function cited above by returning four bytes containing the number of kilobytes free (a more meaningful measure). File Time/Date stamping functions for DateStamper(tm), P2DOS (CP/M Plus compatible), and Joe Wright's NZTIM are all embedded within the Operating System and are concurrently active. While ZSDos2 is still a work in progress, copies are included in the B/P Bios package to allow users to benefit from the newer system. Latest versions were posted in the BPBIOS: directory on the Ladera Z-Node until its demise, and no replacement is yet available. The most recent version of ZSDos2 in 1993 added directory hashing for true speed demons.

Also incorporated in ZSDos2 is a ZCPR34-compliant Command Line Parser. With the permission of Jay Sage, we also modified ZCPR34 to operate in the banked environment, added many common features of Resident Command Processor packages, and simplified it to use the new ZSDos2 Command Line Parser. By folding all features into the CPR, the need for a Resident Command Processor (RCP) extension in high memory all but disappears, typically adding 2k to the TPA.

As a closing note to this first installment, systems using B/P Bios, ZSDos2 and the expanded CPR are currently in operation on the new D-X Designs Pty Ltd P112, Micromint's SB180, a modified SB180 with static memory, two versions of the SB180FX, three YASBEC configurations including a laptop with VGA LCD display, Ampro Little Board (with Terry Hazen's MDISK expansion), and in non-banked mode on a Compu/Time S100 and Teletek. All tools are common across the hardware systems with a complete Z3 Environment and additional segments typically resulting in the equivalent of a "standard" 60k CP/M system. This size is without the RCP typically used to enhance the Command Processor.

The next part of this article will describe the B/P Bios interfaces and standards, while part 3 will cover proposed standards for the evolving ZSDos2, its associated Command Processor and some of the support utilities.

Cameron "Cam" Cotrill is a Senior Software Engineer with Symantec.

Harold "Hal" Bower retired from the US Army Signal Corps in 1990 and has been active in microcomputing since 1976.

Special Feature All Readers

PC Terminal Programs

Program This! The PC Serial Ports

By Dave Baldwin

The Chips

PC serial ports are the result of decisions made in 1980 and never changed since then. The 8250 UART from National Semiconductor was chosen for the original PC's. It is a simple, single-buffered design that is only slightly more advanced than the old AY-5-1013 hardware uart. It has a bunch of extra bus control signals designed to make it 'easy' to interface to just about any CPU. It also has all of the modem control signals available along with two undedicated outputs.

Other designs of the time were double buffered (like the 8251) or triple buffered (like the Z80-SIO) meaning that you could wait longer to read the received characters without losing data. These other chips had limits of their own, however. Neither had all the modem control signals, the 8251 has to have CTS true to transmit and the SIO is designed to work with the Z80 interrupt structure.

Newer versions of the 8250 have been introduced including the 8250A, the 16450, and the 16550. The 8250A fixed a couple of errors in the original chip, the 16450 provided a faster access time, and the 16550 included 16-byte receive and transmit fifos. There are also CMOS versions, the 82C50A and the 16C450. All of them power up to act like an 8250 (almost). The fifos on the original 16550 didn't work, so a 16550A version was introduced with working fifos. 16650 and 16750 versions with larger fifos are also available now from other manufacturers.

The Programs

Two programs are presented here, one in ASM86 and one in 'C'. A third program, SIMPLTRM.ASM will be available on the BBS and the TCJ Web

```
/* SCTERM - Simple C Terminal program, June 1997, by Dave Baldwin
See Issue #80 of The Computer Journal for more info
about this program. Names of the equivalent labels in
     SIMPLIEM and DOSTERM are in parentheses here.
     TCJ Web page: "http://www.psyber.com/-tcj/"
Phone: 800-424-8825
     Written for BorlandC 3.1 */
#include <stdio.h>
#include <dos.h>
#include <comio.h>
#include "SCTERM.H"
#define
#define __CPYANGS
/* prototypes */
unsigned int keychk(void)
unsigned int getkey(void)
void interrupt ( *oldvect)
void interrupt com_isr(__Cl
                                       CPPARGS);/* pointer to save old vector */
(RGS); /* interrupt service routine */
                                 CPPARGS);
                                                   /* get function key cmd*/
/* com-port set up */
/* com-port disable */
void getcmd(void);
void com_enb (void)
void com_dsb (void)
                                                      get receive char from buffer*/
char com in(void)
void com_out(char pch) ;
/* variables */
                                                             /* send char to serial */
                                       /* character from serial port buffer */
char sch
unsigned int kch,kchx;
int xflag = 0;
                                       /* characters from keyboard */
/* program exit flag */
                                       /* old interrupt mask */
/* new interrupt mask */
char int mask
char new mask
unsigned pic_mask = 0x21;
                                        /* 8259 mask port address */
unsigned pic_eoi = 0x20 ;
                                       /* 8259 End-Of-Interrupt port address */
int main(int argc, char *argv[])
/* force value for test */
comp.base = 0 :
    (init01) command line check here */
(argc==2)
      /* check for port number */
     i=0;
k=0;
     while (argv[1][i])
            if (argv[1][i++] != '/')
                   continue;
            portnum = argv[1][i] ;
break ;
     }
```

```
if (portnum=='4')
     comp.base = COM4;
                                   /* (initab) */
     comp.intr = COM4IRQ;
     comp.imsk = COM4MSK:
if (portnum=='3')
    comp.base = COM3;
comp.intr = COM31RQ;
                                   /* (initab) */
     comp.imsk = COM3MSK;
if (portnum=='2')
    comp.base = COM2;
comp.intr = COM2IRQ;
                                   /* (initab) */
     comp.imsk = COM2MSK;
if (portnum=='1')
    comp.base = COM1;
comp.intr = COM1IRQ;
                                   /* (initab) */
     comp.imsk = COM1MSK;
  * défault value *
if (comp.base == 0) {
    portnum = '2';
    comp.base = COM2;
comp.intr = COM2IRQ;
comp.imsk = COM2MSK;
                             /* (initab) */
/* (comptr) initialize address variables for comm port registers */
comp.ier = comp.base+IER
comp.iir = comp.base+IIR
comp.lcr = comp.base+LCR
comp.mcr = comp.base+MCR
comp.lsr = comp.base+LSR
comp.mst = comp.base+MST
comp.scr = comp.base+SCR
comp.baudlo = comp.base;
comp.baudhi = comp.base+1
   initialize memory copies of register values for com port */
creg.baud = 12;
creg.lcr = 3;
creg.mcr = 0x0b;
/* (init03) clear screen, setup serial port and interrupt vector */
clrscr()
com_enb();
/* display signon messages */
cputs(signon);
putch(portnum)
cputs(signon2)
cputs(tcjmsg);
/* (main) ======= MAIN PROGRAM LOOP ======== */
while (xflag == 0)
     /* while the exit flag is zero */
/* check for keyboard input */
    /* check for serial input */
    if (buf tal != buf hed) {
    sch = com_in();
    if (sch) putch(sch);
                                         /* compare head and tail ptrs */
                                         /* get char from serial buffer */
                                         /* display it on the screen */
    }
/* turn off serial port */
clrscr()
cputs(exitmsg);
cputs(tcjmsg);
return 0;
unsigned int keychk(void) {
union REGS regs;
int c;

regs.h.ah = 1; /* check for key ready */

int86(0x16, &regs, &regs);

c = regs.x.flags & 0x40;

c ^= 0x40;
return c;
```

pages. The source code for it is too long to fit in the magazine. I may offer all the code from this issue on a disk if people ask for it.

These programs will work on any PC from an XT to a Pentium and are simple enough that you can modify them for your own uses. The ASM programs (DOSTERM and SIMPLTRM) can be assembled with MASM 4.0 or 5.1, Borland's TASM 3.0, or the public domain Arrowsoft x86 Assembler along with the Val linker. These last two were found on the Dunfield Development web site and are now on the TCJ Web pages and the TCJ/DIBs BBS so you can download them. The 'C' version was done in Borland C 3.1.

Since MS-DOS and the PC BIOS (like CP/M) don't do anything useful with the serial ports, each of these programs does it's own serial port setup. DOSTERM sets up the port for polled operation and uses MS-DOS for keyboard and display. If you have ANSI.SYS loaded, it gives you a very simple ANSI-PC terminal. SIMPLTRM and SCTERM set the port up for interrupt driven operation on receive and polled operation on transmit. This is the only 'universal' setup for interrupt operation. Transmit and status interrupts and bugs vary enough between the chips to require some testing and special handling in the interrupt service routines.

If you decide you want to use transmit and status interrupts, you need to get a copy of 'The Serial Port FAQ' by Christian Blum which is now available on the TCJ web site and BBS. There are problems with transmit interrupts disappearing on some chips and the interrupt response for multiple interrupts is different. An interrupt service routine that takes all of these into account is shown in The Serial Port FAQ and is many times longer than the one I'm using here.

I've put a couple of special 'features' in these programs. The ASM programs are set up so that they will run as EXE or COM programs. I did this when I got tired of having to run EXE2BIN before I could check the results of the next 'newer, better' version. This also helped when I started making larger versions that needed to be EXE only programs. Also, having the three dif-

ferent versions lets you compare what's been done and see the different ways of doing essentially the same thing. I've also tried to kept the names of the routines the same in all three versions so you could compare them. Another thing is that these are all small programs. Even the 'C' version is less than 10kbytes after it's compiled.

All the programs are organized the same way. After defining some values, they check the command line to see if you want COM1 instead of COM2 which is the default port. Then they set up an address table based on the address of the comm port you're going to use, enable the comm port, clear the screen, and put up the signon messages. The 'com_enb' routine is called to initialize the serial port. Since DOSTERM uses the MS-DOS console routines, the 'clear screen' is done as an ANSI escape sequence in the signon message.

Enabling the Serial port

Before you can use the serial port, you have to program the chip and set up the interrupt vector if interrupts are going to be used. SIMPLTRM and SCTERM use the MS-DOS functions to get the old interrupt vector and save it so it can be restored when the program exits and then set the vector to point to their own interrupt service routine, 'com_isr'. Next, all three programs program the serial chip registers to the values needed for operation.

The 8250 family has 9 or 10 addressable registers. The 'Scratch' register doesn't exist on the earliest versions. In ASM86, only the 8-bit I/O addresses from 0 to 255 are directly addressable. For 16-bit I/O addresses, you have to load the DX register with the address and input or output to/from the AL or AX register. Since the 8250 registers are all byte registers, we'll be using only AL.

The first thing we do is to disable all interrupts from the chip while we're programming the rest of the registers by setting IER (Interrupt Enable Register) to 0. Then we send an 83h to the LCR (Line Control Register) to select the baud rate registers. The 8250 has an internal baud rate generator with a 16-bit divider that can divide the baud rate clock with values from 1 to 65535. Divide by 0 is undefined as usual.

```
unsigned int getkey(void) {
union REGS regs;
regs.h.ah = 0; /* get key */
return int86(0x16, &regs, &regs);
void getcmd() {
kchx = kch/256;
                        /* if it's zero, then get extended char */
if (kchx == 68)
                            is it F10? */
     xiflag = -1;
                        /* then set exit flag */
if (kchx == 59)
                               /* is it F1? */
                               /* then clear the screen */
     clrscr() |
    cputs(signon) ;
putch(portnum)
     cputs(signon2)
cputs(tcjmsg)
cputs(helpmsg)
/* COM IN */
char com_in(void) {
char tch
/* get byte from current buffer
                                                 time */
                                            /* return the char from the buffer */
return tch :
/* COM OUT */
void com_out(char pch) {
int cntr = 1000 ; /* time-out counter to prevent lockup */
char tst :
while (cntr-)
                                      /* check time-out counter */
     tst = inp(comp.lsr) & 0x20 ; /* test THRE */
     if (tst)
                                            /* if true, send char */
           outp(comp.base,pch);
           cntr = 0;
                                            /* set loop counter to zero */
    /* and exit */
           break ;
    }
/* COM ENB */
void com_enb (void) {
buf_hed = 0;
                                      /* clear fifo pointers */
buf_tal = 0;
/* save the old interrupt vector */
oldvect = getvect(comp.intr);
/* install the new interrupt handler */
setvect(comp.intr, com isr);
/* disable interrupts while we set up port */
disable();
/* set up serial port registers */
/* set
outp(comp.ier,0);
outp(comp.lcr,0x83);
                                     /* serial chip interrupts off */
                                            /* access baud rate registers *
outp(comp.baudlo,creg.baud);
                                            /* divide by 12 for 9600 baud, low
                                                 byte */
outp(comp.baudhi,creg.baud >> 8); /* high byte of baud rate divider */outp(comp.lcr,creg.lcr); /* set 8N1 */
outp(comp.lcr,creg.lcr);
outp(comp.mcr,creg.mcr);
                                             /* turn on DTR, RTS, and OUT2 */
 * do dummy reads to clear flags */
inp(comp.base) ;
inp(comp.lsr) ;
outp(comp.ier,1) ;
/* re-enable interrupts now */
                                             /* serial receive interrupts only */
enable();
/* set up interrupt mask in PIC */
int_mask = inp(pic_mask);
new_mask = int_mask & (!comp.imsk);
outp(pic_mask, new_mask);
/* COM_DSB */
void com_dsb (void) {
outp(comp.ier,0);
                               /* serial chip interrupts off */
                               /* modem control lines off */
outp(comp.mcr,0)
outp(comp.mcr,v); /* modem cont
/* restore the old interrupt mask */
int mask = inp(pic mask);
new_mask = int_mask | comp.imsk ;
```

```
outp(pic_mask,new_mask) ;
/* restore the old interrupt handler */
setvect(comp.intr, oldvect);
/***NOTE:
     This is an interrupt service routine. You can NOT compile this program with Test Stack Overflow turned on and get an executable
     file which will operate correctly. */
#pragma -N-
                      /* stack checking off */
   COM_ISR */
void interrupt com_isr(__CPPARGS) {
recerr = inp(comp.Isr);
com_buf[buf_hed] = inp(comp.base);
                                                /* read/clear error byte */
                                               /* read data byte */
buf_hed++;
buf_hed = buf_hed & BUFMSK ;
outp(pic_eoi,0x20) ;
                                                /* adjust and mask pointer */
                                                /* send EOI to 8259 */
```

```
/* SCTERM.H - header file for SCTERM.C */
/* COM port and buffer equates *
                                 /* for COM1 */
#define COM1 0x03f8
#define COM1IRQ 0x0c
#define COM1MSK 0x10
#define COM2 0x02f8
                                  /* for COM2 */
#define COM2IRQ 0x0b
#define COM2MSK 0x08
                                  /* for COM3 */
#define COM3 0x03e8
#define COM3IRQ 0x0c
#define COM3MSK 0x10
                                  /* for COM4 */
#define COM4 0x02e8
#define COM4IRQ 0x0b
#define COM4MSK 0x08
#define BUFSIZE 0x2000 /*receive buffer size, must be power of 2 */#define BUFMSK BUFSIZE-1 /* 1 Less for mask */
#define BUFMSK BUFSIZE-1
                      /* Base (No real reason to have this) */
#define BASE 0
#define IER
                  1
                       /* Interrupt Enable Register
                       /* Interrupt ID Register */
/* Line Control Register */
                      2
#define IIR
#define LCR
                       /* Modem Control Register */
#define MCR
                       /* Line Status Register'*/
#define LSR
                   5
                       /* Modem Status Register */
#define MST
                  6
                           /* Scratch Register */
#define SCR
                      /* rts bit in MCR */
#define RTS
                2
                      /* addresses of port registers plus IRQ and mask */
struct comdef {
int base ;
int ier ;
int iir
int lcr
int mcr
int lsr
int mst
int scr
int baudlo
int baudhi ;
char intr
char imsk ;
} comp;
struct COMREG {
unsigned int baud
unsigned char lcr
unsigned char mcr
} creg ;
```

The baud rate registers actually use the same addresses as the data and IER registers, but they're in a different 'bank'. You select the baud rate registers by setting bit 7 or the LCR to a one. The standard PC baud rate clock oscillator is 1.8432 MHz. To get 9600 times 16 (153.6 KHz) you divide by 12. You put 12 in the lower baud rate register and zero in the high register.

Next we load the LCR with 03h which unselects the baud rate registers and sets the chip to 8 data bits, no parity, and 1 stop bit. The MCR (modem control register gets loaded with 0bh for the interrupt version and 03h for polled. The OUT2 bit has to be turned ON in PC serial ports to enable the interrupt gate. This is usually a 74LS125 which is in series with the INTR line from the chip and the selected IRQ line on the bus.

After that, we do some dummy reads of a couple of registers to clear any flags that might have been accidently set. For the polled version in DOSTERM, this is all that's needed. For the interrupt versions, we still have to set the IER to allow receive interrupts and set the appropriate mask bit in the 8259 PIC (Programmable Interrupt Controller).

The disable routine, 'com_dsb', does the opposite of the enable routine. It restores the old interrupt vector and turns off the serial chip interrupts in SIMPLTRM and SCTERM and it turns off the modem control lines in all of them. SIMPLTRM and SCTERM also restore the previous interrupt mask to the 8259.

The Main Loop

The main program loop checks for a keyboard input to see if you want to send anything and then it checks to see if you have received anything. DOSTERM actually polls the serial chip each time. SIMPLTRM and SCTERM check the receive buffer to see if the receive interrupt service routine has put any characters in the buffer.

If there is a keyboard input, it is checked to see if it's an 'extended' char code or a normal character. Normal characters from 1 to 255 are written to the serial

port. Extended codes are checked for the two commands, F1 and F10, that are used by these programs. F1 is the 'help' command which redisplays the signon info and F10 is the exit command.

If there is an input from the serial port, it is sent to the screen. DOSTERM lets MS-DOS handle the control characters and escape sequences while SCTERM let's the video routines built in to the Borland 'C' compiler do it. SIMPLTRM has routines to do the control code and escape sequence processing to emulate the basic functions of an ADM3 terminal and uses the PC BIOS routines for video output.

That's really all there is. Each of these programs can be used as is or easily modified to your own needs. They were left as simple as they are so they would be reasonably easy to understand.

One of the limits on these programs is speed. Don't expect to go above 19.2 KBaud (9600 for DOSTERM) without errors. In 'standard' configurations for PCs, it turned out that everything from a 4.77MHz XT to a 486DX2/66 started getting errors above 19.2Kb. The XT just plain ran out of steam while the background processing caused problems on the 386 and 486. It turns out that background programs like SMARTDRV link into to many of the standard DOS and BIOS routines and use up enough CPU time to limit the interrupt servicing. When I booted a 386 in a minimum software configuration, it would run without error at 57.6Kb with these simple interrupt routines.

An improved version of SIMPLTRM is available for download on the TCJ FTP site and the TCJ/DIBs BBS. Called DIBSTERM.COM, it let's you select which serial port you want to use, tell's you what kind of serial chip the port has, and allows you to change the port while the program is running. It also puts the modem line status at the top of the screen so you can monitor their status and lets you control the outputs with function keys. You can also select the baud rate (from 50 to 115200) and other parameters along with the handshaking mode. It's a good testing program as well as a simple terminal program.

Dave Baldwin

```
DOSTERM.ASM - a simple terminal emulator for PC's TCJ Web page: "http://www.psyber.com/-tcj/"
    Phone: 800-424-8825
    Uses MS-DOS console functions
    Uses the PC serial port in polled mode.
    Can be assembled by MASM 4.0 or 5.1, Borland's TASM,
     or the Arrowsoft public domain assembler and Val linker.
    This is a 'COM' program that can also run as an 'EXE'.
Look for '***' to see what's required to do this.
    There can only one segment, the code (CS) segment.
  EQUATES
false
          egu
               not false
true
          equ
          0dh
   equ
1f
   equ
          0ah
 duplex mode
          equ false
écho
                           ;false = full duplex, true = half-duplex
;standard hardware handshake
         equ 2
                     rts bit in com_mcr
rts
handshake
                     true ;include handshake code if true
               eau
:COM port equates
                     03f8h
ćom1
               equ
                                 for COM2
com2
                     02f8h
               equ
                                 for COM3
com3
               eau
                     03e8h
                                 for COM4
                     02e8h
com4
               equ
  Macros for handshaking routines
  These are used anywhere that video scroll can occur because
   the video BIOS routines turn off interrupts when they scroll.
         MACRO
  rts OFF
IF handshake
    push dx
    push ax
    pushf
    mov dx,com_mcr
         al,dx
al,not rts
    in
                           rts OFF
    and
    out
         dx,al
    popf
    pop
    pop
          dx
ENDI'F
ENDM
ŔTSON
         MACRO
  rts ON
ÍF handshake
    push dx
    push ax
    pushf
    mov dx,com_mcr
         al,dx
al,rts
    in
                           rts ON
    or
    out
         dx,al
    popf
    pop
          ax
         dx
    pop
ENDIF
ENDM
cseg
          segment para public 'CODE'
    org 100h
                                ; COM program
    assume
               cs:cseg,ds:cseg,es:cseg,ss:cseg ;COM program
  sterm proc far ;entry point from DOS
*** set segment reg's for EXE/COM version, all same segment
dosterm proc far
    mov ax,cs
    mov es,ax
                           make SS and ES = CS, leave DS = PSP
    mov
         ss,ax
    mov sp,-2
                            set stack pointer
  *** save psp pointer in real stack along with a '0' push ds ;
    xor
         ax.ax
    push ax
;get command tail
         bx,80h
                           ;point to command line
    mov
                       (uses DS as PSP pointer)
                     get first byte which is char count
         al,[bx]
al,0
                     if 0 (no chars)
    CMD
                           ; use default port (com2)
          inít0b
    jе
```

```
check the rest of the command line
init01: inc bx
mov al,[bx]
                              ;next char
     cmp al,
           init01
                              ; skip spaces
           al,"/"
                               ;first non-space char must be slash
     cmp
           init0b
                                or else use default port (com2)
     jne
                        ;next char
     inc
           bx
           al,[bx]
     mov
           al, ?'
init02
     cmp
                              ;jmp if not '?'
     jne
          dx,offset errmsg; else show 'errmsg'
    mov
     jmp proext
                                  and exit
init02: cmp a. jb init0b
                                    ;is it COM1?
;if not then use COM2
                al,"1"
     cmp al,"4"
jbe init0c
initOb: mov al,"2" ;set default comm number initOc: mov byte ptr com_num,al ;save ASCII comm number ; *** Now set DS = CS because we're done with PSP
    mov dx,cs
mov ds,dx
  set com port address table according to 'com_num' in AL
    call comptr
;put up signon message
init03: mov dx,offset signon
  mov ah,09h
;
                              signon ;get signon message
;display string function
;let dos do it
    mov
int
          21h
          dl,byte ptr com_num ;get comm number
ah,06h ;display char function
    mov
    mov
                              ;let dos do it
    int
          21h
                              ;get signon message
;display string function
;let dos do it
           dx,offset signon2
    mov
    mov ah,09h
int 21h
                              ;start up communications port
    call com_enb
    Main program loop
mov_dl,Offh
main:
    mov ah,6
int 21h
                       ;direct input
                       ;ask DOS for keyboard input
;no char, skip
;is it extended key code?
; Yes, go process
          main4
     jΖ
    cmp al,0
          main5
    j e
main2:
    if
         echo
                       ;if running half-duplex, echo char
; to PC display
    push ax
    call vidout
    pop ax endif
    call com_out
(com_inp) check if char waiting at comm port
main4:
                              ;get receive status
    mov dx,com_lsr
          al,dx
    in
                        ;check receive data ready flag
    and al,1
                       ;no, loop
    jΖ
          main
                              ;data port
    mov dx,com_base
    in al,dx call vidout
                              ;write it to PC display
                              ;see if any more waiting
    jmp main4
  check function keys
main5:
;get second byte mov dl,Offh
                       ;direct input
                       ;ask DOS for keyboard input
    mov ah,6
int 21h
cmp al,59
jne main6
; F1 (Help) message
RTSOFF
                              ;F1?
                                    ;get signon message
    mov dx,offset signon
                              ;display string function ;let dos do it
    mov ah,09h
int 21h
```

References:

Advanced MS-DOS Ray Duncan Microsoft Press

ASM and C programs for MS-DOS. I started out by copying the TALK.ASM program from this book.

The Peter Norton PC Programmer's Bible Norton, Aitken, Wilton Microsoft Press

The 'standard' refence for beginning and intermediate PC programmers.

MS-DOS Programmer's Reference, Version 5 Microsoft Press

Extensive listing of all the MS-DOS functions with short sample routines and all of the structures used by MS-DOS up to version 5.0

The_Serial_Port_FAQ Christian Blum

Look here for routines for detecting and using the 16550 uart with fifos for high-speed communication. Available on the TCJ FTP site.

National Semiconductor Data Communications Handbook

8250 thru 16550 data sheets. Also available from their web site as Adobe Acrobat PDF files. "http://www.natsemi.com"



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INS8250 40 □ vcc D0 □ ☐ /RI D1 🗀 2 39 D2 🗆 3 38 ☐ /DCD D3 🗆 37 ☐ /DSR 4 36 🗀 /CTS D4 🖂 5 35 🗀 MR 6 D5 🖂 D6 □ 34 🗀 /OUT1 7 33 🗁 /DTR D7 🗀 8 32 9 □ /RTS RCLK 🖂 10 31 | INTR ☐ /OUT2 SIN = 30 SOUT = 11 12 29 □ NC CS0 □ 28 CS1 □ 13 □ A0 27 🗀 A1 /CS2 □ 14 /BAUDOUT ☐ 15 26 🗀 A2 25 🗀 /ADS XIN 🗀 16 XOUT 🖂 17 24 CSOUT MR □ 18 23 DDIS 22 🗀 RD WR 🖂 19 20 21 □ /RD vss □

```
Pins:
 1-8
       D0 thru D7, data lines
 9
        RCLK - Receiver clock
 10
       SIN - serial input
       SOUT - serial out
 11
 12-14 CS1-3 - chip selects
       /BAUDOUT- Oscillator
 15
       output
       XIN - crystal input
 16
       XOUT - crystal output
 17
 18-19 WR - write control
       VSS (gnd)
 20
 21-22 RD - read control
 23
       DDIS - driver disable
 24
       CSOUT - chip select out
       /ADS - address strobe
 25
 26-28 A0-A2 - address lines
       NC
 29
 30
       INTR - interrupt output
       OUT2 - used to enable PC
 31
       interrupts
 32-34 Modem/control outputs
      MR - Master reset
 35
 36-39 Modem/control inputs
       VCC - +5V
 40
```

```
mov dl,byte ptr com_num ;get comm number
mov ah,06h ;display char function
int 21h ;let dos do it
    mov dx,offset signon2 ;get signon message
mov ah,09h ;display string function
                          ;let dos do it
    int
        21ĥ
    mov dx,offset tcjmsg ;restore message pointer
mov ah,09h ;display string function
int 21h ;let dos do it
    RTSON
main5m:
    RTSOFF
    mov dx, offset errmsg
                                ;get message offset
                         display string function; let dos do it
    mov ah,09h
    int
         21h
    RTSON
    jmp main
main6:
         cmp a1,68
                         ;F10?
                    ;yes, exit
;if not, ignore and loop back to 'main'
    je mainx
jmp main
         mainx
         mov dx,offset exitmsg ;print farewell message
mainx:
exit procedure
prgext:
; *** set DS in case of error exit
    mov ax,cs
    mov ds,ax
    mov es,ax
                    ;save message address
    push dx
                    disable controller and release int vec
    call com_dsb
    pop dx
;
         ah,9
                    ;let DOS print message
    MOV
    int 21h
   mov ax,4c00h ;exit with ret code = 0 int 21h
                    ;far return just in case
;just in case
    ret
    int 20h
dosterm endp
vidout proc near ;write char in AL to display
 mov dl,al
mov ah,6
                    ;use DOS DIRECT console
                    save bx
   push bx
        21h
    int
   RTSON
   pop bx
   ret
vidout
        endp
send char in AL to serial port
com_out proc near
   push ax
   push ax ;save char
mov dx,com_lsr ;check tbe stat
mov cx,2000 ;anti-lockup
com_out1:
   in al,dx
and al,20h
jnz com_out2
loop com_out1
                   THRE; send if ready; loop until ready
                    restore char
   pop ax
   ret
com_out2:
   pop ax
mov dx,com_base
   mov dx,com
out dx,al
                         ;write char to port
com_oxt:
   ret
com_out endp
set up comm port
com_enb proc near
                 er ;interrupt enable register ; no interrupts
   mov dx,com_ier
mov al,0 ;
   out dx,al
   mov dx,com_lcr
                         ;set line control
   mov al,83h
                         ;select baud reg, set parms below
```

```
out
        dx,al
                        ;set 9600 baud
;lo byte
   mov
        dx,com_base
        al,Och
   MOV
        dx,al
   out
                   ;point to high byte
   inc
        dx
                        ;high byte is 0
        al,al
   xor
   out
        dx,al
 set r/t parms
        dx,com_lcr
   mov
                        unsel baud reg, no parity, 1 stop, 8 bits
        al,03h
   mov
   out
        dx,al
                        ; modem controller DTR, RTS,
   mov
        dx,com_mcr
   mov
        al,03h
   out
        dx,al
                        ;dummy read of serial port
   mov
        dx,com_base
                        to clear flag
   in
        al,dx
   nov
        dx,com_lsr
                        dummy read to clear stat flags
   in
        al,dx
com_enb endp
 turn modem control outputs off
com_dsb proc near
        dx,com_mcr
                  ;turn off all mcr outputs
        al,0
        dx,al
   out
   ret
com_dsb endp
 -------------
 gets base pointers and updates I/O address table
        proc near
comptr
        bx, offset port1
                             :offset to port1
   MOV
   CMD
        al.
         comset
   jΖ
        bx,offset port2
                             offset to port2
   ňον
   CMD
        al.
   jΖ
         comset
        bx, offset port3
   mov
                             offset to port3
            12
   cmp
        al.
         conset
   įΖ
        bx, offset port4
                             offset to port4
   ňov
   CMD
        al,
        comset
        dx,offset errmsg ; EXÍT because no COM specified.
   mov
   xor
        ax,ax
   ret
;load I/O address table for selected com port
comset:
                        ;get base
   mov
        ax,[bx]
                             ;check for zero
   or
        ax,ax
        comptx
                             ;zero error exit
   jΖ
        word ptr com_base,ax
   MOV
        ;+1 for ier/baudhi
word ptr com_ier,ax ;
word ptr bandhi
   inc
   mov
        word ptr baudhi,ax
   MOV
   inc
        ax
                        +2 for lin
   inc
        ax
        word ptr com_lcr,ax;
ax ;+1 for mcr
   MOV
   inc
        word ptr com_mcr,ax;
                        ;+1 for stat
   inc
        ax
        word ptr com_lsr,ax;
ax ;+1 for mst
   inc
   mov
        word ptr com_mst,ax ;
comptx:
comptr
        endp
            com port address assignments
                       ;port address
port1
        dw
             com1
port2
              com2
                        ;port address
                        ;port address
port3
        dw
              com3
port4
              com4
                        ;port address
```

More advanced programs

In more complete terminal emulations and file transfer programs, the serial code is a small part of the program. Terminal emulations require direct video routines because the PC BIOS routines are inadequate and too slow, file transfers require a lot of code for the different protocols, and both require code to control the modem.

There are several other problems that need to be dealt with on PC's. You may need a 'CPU ID' routine to tell you what kind of machine your program is running on. Plain PCs and XTs only have the low order interrupts available (IRQ0-7) while the AT/386/486/Pentiums have IRQ's 0 thru 15 available. If your program needs to be able to use high order IRQs (9-15), you will need a slightly different interrupt service routine for your receive interrupt.

On a PC, you also need to provide a 'Critical Error Handler' routine so that disk file problems don't crash your program. The 'default' action of the Critical Error Routine (Abort, Fail, Retry?) will abort your program and return to DOS if you don't provide a routine that gives your program control.

You also need to 'intercept' the timer interrupt to eliminate software timing loops. Since fixed software timing loops will run at drastically different rates on different PC's, using the timer interrupt will allow you to have consistent timing on different machines.

Another problem is 'handshaking' on the serial ports. Handshaking is used to start and stop the flow of data to allow the programs to do something else for a moment like reading or writing files or scrolling the screen. DOSTERM shows very simple hardware handshaking (RTSOFF/RTSON). Some situations require other modem control lines for handshaking and there are several different kinds of software handshaking.

And then there's modems. They have to be sent 'AT' command strings in the proper order and you have code to recognize the responses to know what to do next. TCJ #79 has David Goodenough's article on the AT modem commands.

cseg ends

end dosterm

8250 Register Addresses

	0	0	1	2	3	4	5	6	0	1
		DLAB=0	DLAB=0						DLAB=1	
	RECV	TRANS	Interrupt	Interrupt	Line	Modem	Line	Modem	Divisor	Divisor
register	buffer	holding	Enable	ID	Control	Control	Status	Status	Latch	Latch
bit	register	register	register	register	register	register	register	register	low	hi
				101 :6	Word	DTR	Book	Delta	Bit 0	Bit 8
0	DB0	DB0	Recv	'0' if	Length	אוט	Recv Data	CTS	Dit 0	Dit 0
			data available	Interrupt pending	bit 0		Ready	010		
			avallable	pending	Dit 0		Ready			
1	DB1	DB1	Transmit	ID bit 0	Word	RTS	Overrun	Delta	Bit 1	Bit 9
•	55,		holding		Length		error	DSR		
			reg		bit 1					
			empty							
2	DB2	DB2	Recv	ID bit 1	Number	Out1	Parity	Trailing	Bit 2	Bit 10
			Line		of Stop		error	edge		
			Status		bits			Ring		
						0.40	Francisco	Indicator Delta	Bit 3	Bit 11
3	DB3	DB3	Modem	0	Parity	Out2 (PC INT	Framing	Delta	DILO	DILII
			Status		Enable	enable)	error	DCD		
						enable)				
4	DB4	DB4	0	0	Even	Loopback	Break	CTS	Bit 4	Bit 12
~					Parity		Interrupt			
		:		,	Select		-			
]							
5	DB5	DB5	0	0	Stick	0	Transmit	DSR	Bit 5	Bit 13
					Parity		Holding			
			<u>.</u>			-	register			
							empty		Diac	Bit 14
6	DB6	DB6	0	0	Set	0	Transmit Shift	Ring Indicator	Bit 6	DIL 14
	•				Break		register	inuicator		
				}			empty			
7	DB7	DB7	0	0	Divisor	0	0	DCD	Bit 7	Bit 15
7	067		"		Latch		_			
					Access					
j					Bit					
					(DLAB)					
<u> </u>	1		·		<u></u>					

Real Computing

By Rick Rodman

32-Bit Systems

All Readers

Real-time Control

August in the Nation's Capital: ragweed pollen floats in the hot, sticky air. Gnats and mosquitos greet them that dare venture out from air conditioning and HEPA filter. It is a time for reflection, for contemplation of possibilities, for antihistamines, most of all for staying inside.

The Timer

As an old saying goes, when life hands you a lemon, make applesauce. Many times we look in the wrong place for a solution to what is really a simple problem. Part of my plans and thoughts regarding my Real-Time Control System center around avoiding utility waste, and one of my pet peeves is lights being left on - particularly in the basement, but also in bathrooms. This has led me to try various timer devices, X-10 modules, timer controllers, and RTCS. But now I've found a much simpler solution.

This is a device available from Marlin P. Jones Associates, called a "SSAC TS120A-966 Solid State Timer", which the catalog says "supplies 115VAC@1A max to the load for 30 min. then power is removed from the load". What it really does is, it turns off lights after 30 minutes. (Sorry, no shorter durations are available.) It does the job perfectly, it's simple to connect and it costs only \$3.75.

The MPJA catalog is a candy store for experimenters, full of neat optoelectronics, power supplies, unusual switches, connectors and other exciting stuff. Maybe I'll finally get around to building the Chaos-Pandemonium Box.

Newton

As the Chinese say, a journey of a thousand miles begins with a single stumble. Some readers will remember Apple's other personal computer, the Newton, with its crummy handwriting-recognition technology. The Newton not only cost \$800, but it required a souped-up Macintosh and an expensive development kit even to do the simplest programming and, on top of all that, used its own proprietary language, a very weird object-oriented dialect called NewtonScript. In management, and in baseball, they say a project can survive one big mistake, might survive two, but three strikes and you're definitely out.

Well, now that monied interests have moved to greener pastures, there remains fertile ground for enjoyable experimentation. Used Newtons are available cheaply - sure, they're not the latest models, but there haven't been that many changes in the line. Better yet, an inexpensive development tool is available, Steve Weyer's Newt. Newt, and its companion Slurpee, let you do typing on a PC - or a Sun or Kaypro or anything at all, really - and compile on a Newton.

Once you realize that a Newton is not suitable for any significant data entry, you start thinking that there's a lot of stuff that'd be really neat to do. One thing I want to do on it is for my car, to keep records, perform milage calculations and remind me about oil changes.

A CD of Newton programs is available from AMUG. While there appears to be no source code on this CD whatsoever, there are plenty of programs, mostly shareware, which may do what you want to do. In fact, one program, called MPG2, does exactly what I described in the previous paragraph.

Apple Computer recently released a beta of the long-anticipated Newton Toolkit for Windows, which actually requires Windows 95 or NT, and you can download it from their Web site.

Probably I won't write much more about Newton topics unless our esteemed editor prompts me, but for the TCJ reader the relevant facts are: ARM RISC processor, 128K to 512K of internal RAM, 1, 2 or 4MB flash card, graphic display with stylus input, no disk or keyboard, one RS-232 serial port.

Java

They say you can lead a gift horse to water, but don't look him in the mouth. From an informal survey of books in local bookstores, it looks like Java is far and away the most popular programming language today, outpolling Visual Basic and C++ combined. So what is it? It's a compiler/interpreter, like BASIC-E, CBASIC, and UCSD Pascal. A web page containing an "applet" causes a browser to request that "Java Byte Code" (p-code) be sent, where a "Java Virtual Machine" (interpreter) runs it. Nothing particularly innovative about that, is there? Of course it has the usual object-oriented stuff like classes and methods that are de rigeur these days.

While people always rush to say "it's a lot like C++", this is

not true. It has none of C++'s hard-to-read double colons or overloaded operators or templates or virtual functions, features which nobody in their right mind would use anyway. Some of its declarations look more like Pascal.

The most important difference between Java and C or Pascal is that Java doesn't have any pointers. Although pointers use a quirky syntax in C and are a minefield for the unwary, they are actually the language's most powerful feature. Without pointers, we're reduced to pass-by-reference/pass-by-value, like we had to do way back in the Fortran days. In fact, because of Java's syntax, I think the best alternative name for it is... Object Ratfor.

Microsoft's motto is "Good things come to those who waste", and they hope to crush Java in their deadly embrace. They have announced a package called "Visual J++", which is a version of Java modified to support what are now called "Active X Objects" (formerly called "OCXs" and "OLE Custom Controls"). The name "J++" is supposed to look like "C++" (repeating the mistake that name makes), but Microsoft, in their usual narrow vision, didn't notice that there is a very popular language called J, a derivative of APL. Anyway, Visual J++ looks like a package that can be safely avoided.

In Windows 95 and in NT version 4, the once small, quick Write word processor, which has been getting bigger over time, is replaced by a new program called WordPad. From what I can see, it has nothing that Write didn't have. But now, thanks to Microsoft's "dogfooding", it uses MFC and takes ten times as long to load. Efficiency is evidently a dirty word at Microsoft. I wonder if Bill Gates, the hotshot programmer who cajoled a full BASIC interpreter into the Altair's limited RAM, knows or cares what schlock his minions are producing.

More on Small-C for embedded systems

Frank Wilson writes to say that he has used CUG 6809 Small C to do work on a Color Computer and on a small 6809 SBC, and fixed a lot of bugs in it. "The 'logical not' code generation portion screws up the stack. Also, I think the integer divide had a sign problem. Eventually the darn thing would self compile on the CoCo, and I also got it to compile on a 68HC11." He also says: "Maybe using a PC for cross development is cheating, but it simplifies things and makes fooling with obsolete processors a low cost option." I don't think it's cheating, Frank. After all, a PC has to be good for something, doesn't it?

He also mentions some cross assemblers which are on CUG's CD. Most of these are fairly crude. The ones I like best are the Frankenstein cross assemblers. When working with assembly code, what can seem very minor syntax variations can just drive you crazy, especially when it comes to macros. In the Unix world these things are often standardized, but in the wild-and-woolly PC world, you never know what to expect.

You've seen the movie, now get the OS

The Plan 9 distributed operating system, named for the movie "Plan 9 from Outer Space", is available from AT&T in source code form for \$350.

Next time

The RTCS becomes more truly real-time as it meets the TW-523 X-10 interface and the Watson voice card. Plus, time and space permitting, the difference between 'sound' and 'voice' and how to overcome it. Remember, it's not what your computer has, but what you can do with it!

For more information

Kettle Pond Computing Facility BBS or Fax: +1 703 759 1169

E-mail: ricker@erols.com

Mail: 1150 Kettle Pond Lane, Great Falls VA 22066-1614

Marlin P. Jones Associates: 1 800 652 6733 or +1 561 848 8236 Timer, item # 4381-RL, \$3.75 P.O. Box 12685, Lake Park FL 33403-0685

Steve Weyer (Newt Development Environment, etc.) weyer@netaxs.com 17 Timber Knoll Drive Washington Crossing PA 18977

AMUG CD Inc. (Totally for Newton CD #6, \$24.95) +1 602 553 0066 or -0144 fax 745 N. Gilbert Road #124-275, Gilbert AZ 85234

AT&T (Plan 9 operating system, \$350): +1 908 577 2700 2 Paragon Way, Suite 400 Freehold NJ 07728

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Cheap Hard Disk Controllers

by Allison Parent

Special Feature 8085 to PC-ISA

Hard Disk Interface

Adapting a PC/ISA card to an 8085.

I needed a hard disk for a 8085 project. The common solution is to use a host interface and controller. However, boards like the WD1002HDO are becoming scarce. I considered SCSI but I'd need a SCSI interface to drive a SCSI drive and I didn't have either of these either. I opted to look at a different source for a hard disk controller for my 8085 board. What I was trying to avoid was complex interfacing and spending money. The most obvious source was cheap and plentiful supply of 8bit ISA bus cards. I settled on the WD1002S-WX2A mostly because I had two that were good. They would interface to the ST225 and ST251 drives I have laying around.

The question is, what does it take to talk to it? That was helped along when a request for information yielded an article interfacing the slightly smaller WD1002S-WX1 to an SC84 Z180 system. The WD1002 ISA boards are interchangeable for the application, the only differences being board size and surface mount instead of dips. The next step was creating a 8085 to ISA 8bit adaptor. I had several articles that described this in painful terms. I didn't need the ISA bus for general use, I just wanted a hard disk controller. I rejected creating a copy of the ISA bus as being too complex. What I wanted was the 1002HDO! The problem was, how do I make the 1002S-WX2A look like a few simple ports to the CPU?

Going to the drawing board, I pulled out one of the boards and started looking at it closely with the specifications that I had available. It was a complete controller. The interface is fully decoded, buffered and it requires a known set of TTL compatible signals from the ISA bus. Without schematics for the card, it was, for all intents, a black box. Actually this is ok since we know what the inputs and outputs are and what goes on in the middle has been done for

The 1002S-WX2A responds to a standard address for I/O at 320h to 323h and has Eprom at C8000h to C9FFFh with the standard jumpers in place. The control signals were address, MemRD/, IORD/, IOWR/, DRQ, DACK, IRQ, AEN and Reset. Right off, I could see that this was a subset of the ISA bus which cut the interface task down some. Looking at the card in hope of getting some inspiration, I no-

ticed that on the edge connector many bus signals did not even have contacts. An idea, how much of the interface could be eliminated? First off was the Eprom at C8000h. The system has enough Eprom of it's own and clearly this was excess. This eliminated the MemRD\ and A10 through A19. This was a start. I then looked at how to put the board into an eight bit address space.

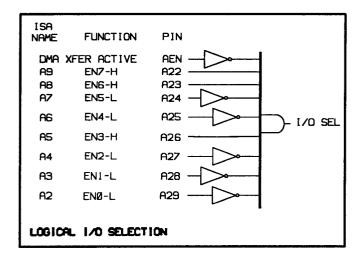


Figure 1 Logical I/O selection.

Looking at the I/O address space control lines made several things obvious. Addresses A0 and A1 are register selects. I guess-timated that somewhere on the board or in a chip the remaining eight lines enable the board for I/O. The likely decode is shown in the figure as the logical And of those eight lines, five are active low and three active high. We only need 6 of these lines to select an 8 bit address. By selecting from the available enables and forcing the unused two to zero or one as needed we can have the board appear at many different addresses. I chose to use the two active high and four active low to assign the board to C0h. The remaining active low line is grounded.

I used one of the active high lines to qualify IO operation selection off the 8085 IO/M\ line. The 8085 board does not fully decode IO/M\, RD\ and WR\ to distinct IORD\ or IOWR\. The same idea could be used in a Z80 system to decode the IORQ\ and RD\ or WR\. I decided to connect the HDC reset line to the 8251 DTR\ line as a convenient

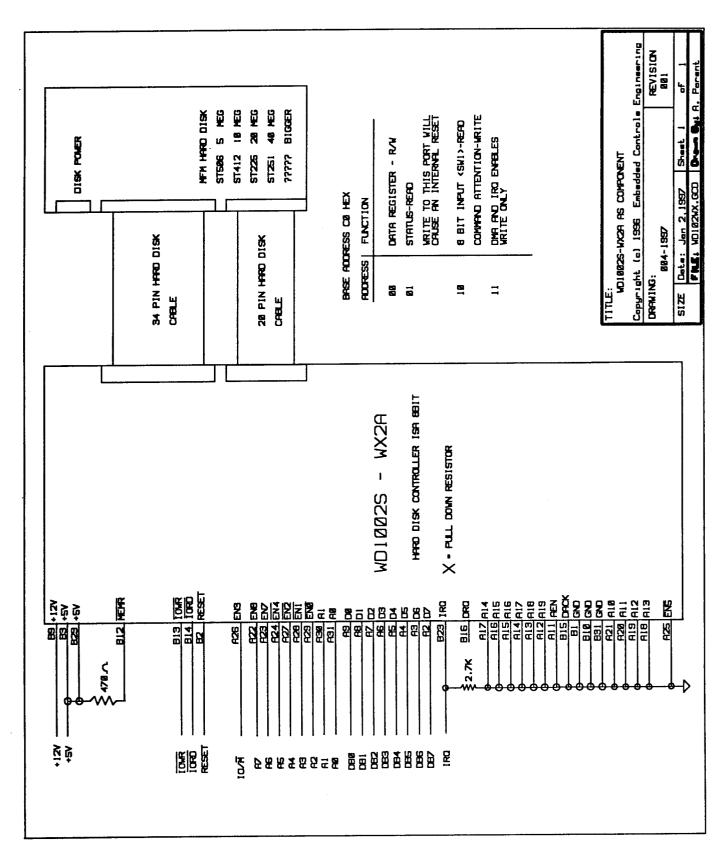


Figure.2 Pinout of the WD1002S-WX2 as component with interface names

```
; Header file for HDC
   Assemble using DRI ASM or equivelent.
   SIM and RIM will be inserted with DB.
                               : insert as DB SIM
; insert as DB RIM
                    20H
 RIM
            EQU
   PROTO test bed card is Vt100 Printer Buffer Card These are slightly 8085A, with 4k EPROM. 2k RAM, 3 8251As, 8116 BRG and minimal glue logic.
   Mods applied are freeing up interrupt pins,
Supplying BRG output to all 8251s and adding
   local reset generation
   Here we keep all the important addresses for code and whatever.  \\
   Memory locations:
                    0000
                               ; ROM starts at 0000h
ROM
            EQU
                    1000H ; ROM is 4k part
2000H ; Memory decode is 4k boundary
0800h ; RAM is 2k part
             EQU
ROMLN
            EQU
RAM
RAMLN
            EOU
   Magik memory addresses:
   Interrupts in hardware of 8085A. The RIM and SIM
   instructions can monitor status of and mask interrupts.
                              : Level trigger maskable priority 4
: Level trigger maskable priority 3
ÍNT55
                    02CH
                    034H
            EQU
INT65
            ĒQŬ
                    03CH
                               ; Edge trigger maskable priority 2
INT75
TRAP
                               ; non-maskable high priority 1
            EOU
                    024H
:IO decodes:
                             ; data port 8251 device A
; CSR for 8251 device A
; Data port 8251 device B
; CSR for 8251 device B
OH ; Data port 8251 device C
; CSR for 8251 device C
; base address for BRG
PORT51A EQU
                    000
                    010H
020H
CSR51A EQU
PORT51B EQU
                    030H
CSR51B
             FOU
PORTSIC EQU
CSR51C EQU
                          040H
CSR51C
                    050h
BAUDB
            FOU
                    060H
  The low 4 bits are baud rate.
Baud rates below 1200 left off for brevity
All ports use same BRG!
                                                baud rate
                    Address =
 :Name
B1200R EQU
B2400R EQU
B4800R EQU
                                    ; 16x 1200
                    BAUDB+12
                                    : 16x 2400
: 16x 4800
                    BAUDB+13
                    BAUDB+14
                                    ; 16x 9600
B9600R EQU
                    BAUDB+15
                                               : 16x 19200
B1920R
            EQU
                    BAUDB+16
; 8251A CSR Bits.
   Command bits
                   ts 100000000B ; Not used, sync mode 01000000B ; internal reset 1=reset 00100000B ; 1 sets RTS pin to 0 00010000B ; Error Reset 1=reset 00001000B ; a 1 Forces TX break 00000100B ; RX enable 1=enable 00000010B ; 1 sets DTR pin to 0 00000000B ; TX enable 1=enable
ÉNHUNT EQU
IREST
RTSF
ERES
            FOU
            EOU
            EOU
SBRK
            EOU
RXE
            FOU
DTRF
            FOU
                    00000001B ; TX enable 1=enable
TXEN
            EQU
NOMCWD EQU RTSF+ERES+RXE+DTRF+TXEN ; typical CSR byte
  Note CSR51A DTR is used to control hardware reset of the HDC
  should it get lost and at power up. CSR51A must have DTRF set to 1 to clear HDC reset. This will be done in the general INIT code that sets up board level and branches to HDCinit.
; Status bits
ĎSRS
                    10000000B ; DSR status
            EOU
                    01000000B; SYNC det, sync mode
00100000B; Framing error
SYNDET
            EQU
FERR
            FOU
ORERR
                    00010000B
                                       Overrun error
            EQU
                    00001000B; Parity error
00000100B; TX empty
00000010B; RX reg has char if 1
PERR
TXEM
RXRDY
            EQU
            EOU
            FOU
                    00000001B; TX reg can accept char if 1
TXRDY
            EQU
```

and controllable single bit port. I may add that the DTR\ goes high at power on reset time so this give me a power on reset as well. This makes it possible to do a software reset of the HDC.

Further simplification was found by choosing to not implement DMA. This meant ignoring the DRQ line and forcing the DACK line to the false condition. Data is buffered on the controller card so DMA to keep up with the disk is not required. I did hook the IRQ line to the RST5.5 line on the 8085 for later interrupt use because it can also be polled using the RIM instruction. This means a polled transfer. Also lines like AEN had to be forced to false to prevent spurious deselects. AEN is used during DMA data transactions to disable the address selection logic as the DMA controller does this with the DACK signal. I might add that IORDY and IOCHK\ on the ISA bus were not used by the board. For initial testing, this is easier to debug.

See Figure 2 for the pinout of the WD1002S-WX2 as component with interface names

The target system is something I have a bunch of. They are printer buffer cards for vt100 terminals. Their basic design is 8085, 4k of eprom, 2k of ram, 3 8251 usarts with rs232 conversion and a single band rate generator. This, with minor mods, is useful for control systems on a card that is 4.5 by 5 inches. I have a simple debug monitor with download to use on this board. It's simple and general enough in design to use for anything. This was a suitable platform to test the interface to the HDC. Other possibilities could have be 8748/9 or 8751 single component CPUs. The obvious use is on a CP/M system that needs a hard disk interface.

The interface at this point is all mechanical and interconnection to the 8085 board. The 8085 board does not have a external bus but it's easy enough to pick up the needed signals directly off the 8085 and 8251. Some would complain that I may have exceeded the fanout of the 8085 but the 3mhz part has good output drive and fairly relaxed timing. The board, drive, and controller used the same power supply since

it was big enough. Testing has progressed to the point where the interface responds and drive seeks were performed by poking data to the various ports. Programming is the next aspect of the project and is a later article.

The idea that a PC ISA bus card can be applied to systems other than PCs is not new. In most cases the goal was to create a complete bus so any card could be used. While that approach has value, it is also far more complex. As another possible application, I looked at a modem card and again saw a simplified interface that would lend itself to other applications as a black box component. My goal was to find a hard disk interface cheap. By examining a widely available PC hard disk controller and equating it to a large chip essentially made the board usable for non-PC applications. Also, there are many hard disk boards for ISA that appear the same or very similar. This would make replacements easier to come by.

Allison J Parent <allisonp@world.std.com>

```
; HDC IO:
                    OCOH ; base address of controller
HDCB+0; HDC data register bi directional
HDCB+1; HDC status read
HDCB
             EQU
DATAR
            EQU
STATS
            EQU
                NOTE: A Write to STATS causes internal reset
               OU HDCB=2; Eight bit input, reads setup sw
NOTE: A Write to EBIR causes a command attention
EBIR
             EQU
DMAIRQ EQU HDCB+3; DMA and IRQ enables write only
   DMAIRQ bits
   Even though they may not be used at the bus level they must be
   enabled for status IO via STATS read.
                               ; Enable DRQ external request and status bit : Enable IRQ external resquest and status bit
                    01B
                    10B
TROFN
            FOU
  commands are packet oriented. The host will first write to EBIR to force the controller to command attention for a command write when REQ is asserted the host will then write a multibyte command block via DATAR. Monitoring the status of STATS register is required for protocol handshake.
  HDC port read bits for STATS
             EQU
                          00100000B
                                                     ; interrupt request
HDIRQ
            EQU 00010000B; DMA request
EQU 00001000B; controller is executing a command
EQU 0000100B; Command or data
; Indicates a data transfer <1> or status<0>
EQU 00000010B; IO direction
DMARQ
BUSY
CDSTS
IOSTS
               Indicates direction of transfer read if set, write if clear
    ; Controller is ready for data transfer if set Host buffer
            EQU 00000001B ; Request
REQST
                     RAM
                               ; at start of RAM
             ORG
SECBUF
           DS
                     512
   Command buffer
  Some commands allow 11 bits for cylinder address, the largest value allowed is 1024 (10 bits). Number of heads are limited to 8. Sectors per track is 17 invarient. A sector is 512 bytes. The largest drive is then 1024*8*17*512=71mb
                                ; Command code
HITCHIO DR
                               ; bit 5 drive, bits 4-0 head number
; bits 7-5 MSB of cylinder number
                     00
HDCMD1 DB
HDCMD2 DB
                     00
                                  bits 4-0 sector number
                                : LSB low 8 bits of cylinder number
: Sector count or interleave (command dependent)
HDCMD3
             DB
                     00
HDCMD4
            DB
                     00
                               ; bit 7 retry disable, general retry
; bit 6 retry disable, ECC retrys
HDCMD5 DB
                                ; bits 2-0 step rate
                                    000=3ms, 100=200us, 101=70us
```

ÉND

Simplex III

Part 3

by Dave Brooks

Special Feature
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TTL Computer

Simplex-III Machine Instructions

This is the third in a series of articles decribing Simplex-III, a home-designed CPU. The machine was built in the late 1970's, using discrete TTL parts. Simplex-III was a big-endian machine, with the least-significant byte of a multi-byte object at the highest address. Data width was 8 bits, with a 64kB address space.

The overall architecture was described in the previous issue. The programmer-visible registers are shown in Table 1. These registers were implemented in a small bipolar RAM, the "SPAD".

<u>Table 1</u> Name		BytesAddress Function				
s	2	01	Sequence (instruction pointer)			
X1	2	23	Index / data register			
X2	2	45	ditto			
ХЗ	2	67	ditto			
Α	18	8F	Workspace (accumulator)			

A typical instruction proceeds by reading the S register (in 2 bytes) from SPAD, incrementing it by 2, and posting the result back to SPAD and to the two bytes of the Store Address register. Two memory-read cycles follow, with the 16-bit address register auto-decrementing each time.

Since all instructions are 2 bytes long, this leaves the operation-code in the Instruction Register, and the address offset in the "R" register (a temporary register). The 8 instruction bits are broken (in most instructions) into 3 fields thus (recall that in big-endian notation, bit-0 is the most significant):

Operation	4 bits [0:3]
Operand register	2 bits [4:5]
Index register	2 bits [6:7]

The first operand is selected by the "operand register" bits, as A, X1, X2, or X3. The second operand is addressed in memory, by zero-padding the content of "R" (the address offset), and adding the content of the "index register" S, X1, X2, or X3. As before, this addresses the highest (least-significant) addressed byte of the operand. As the operation proceeds, both the memory and SPAD address registers auto-index.

Relative jumps are executed in the same way, by taking an address forward or back relative to S, and storing that address in S. The 8-bit displacement is always zero-filled to 16 bits: an instruction bit determines whether this value is to be added or subtracted from the S register.

For all registers except A, the data length is fixed at 2 bytes. A "length" register can be loaded, to define the length of A at anything from 1 to 8 bytes. Of course, this value simply defines the repeat count for operations involving A. The length value remains set until changed explicitly changed again.

A typical instruction is:

ADD A,X1,DATA

where "A" is the operand, and "X1" the address base. "DATA" is the address of the second operand, as an offset from register X1. The effect of this instruction is to add A (at the currently set length) and DATA, storing the result in A. The condition bits will also be set.

Instruction-bytes take one of the 4 formats listed in Table 2. All instructions use Format 1, except for the SET and BC instructions.

```
Table 2: Instruction Formats

Format — Function Byte —

0 1 2 3 4 5 6 7

1. -Op-code— -Ro- -Rx-
2. 0 Length
3. 1 IT J K
4. Condition Dirn.
```

Formats 2 and 3 are used by the SET instruction. When I[4]=0, the remaining bits set the effective accumulator length to 1..8 bytes, giving a working (integer) precision of 8..64 bits. When I[4]=1, I[5] terminates an interrupt, while I[6:7] are the J and K inputs to a flipflop. This flipflop drives a "signal" LED as a prompt to the user. SET instructions ignore the address/data byte. This instruction is not used often enough to justify the extra logic to count S by only one byte, and so save the space taken up by the address byte.

Format 4 is used by the Branch Conditional instruction. If I[7]=0, the address offset is added to S for a forward branch, while if I[7]=1, the offset is subtracted, for a backward branch. I[4:6] determine the branch condition, as shown in Table 3.

The machine instructions are listed in Table 4. The JI/JIL instruction has a side-effect, in that if Ro=X1, X2, or X3, S is stored in Ro (ie save subroutine link). If Ro=A, the link is discarded (ie the instruction is a simple jump). Then or otherwise, q => S (indirect jump). If this instruction is executed in interrupt level, both S registers are loaded: this intentional side-effect was used at boot-up to set up the interrupt vector (the interrupt-level S register) as explained below.

Subroutine return is typically done using the "MIR" (move & increment register) instruction. This takes a 2-byte register, adds a constant, and stores the result in the same or another register. A typical subroutine entry/exit sequence is listed in Table 5, where the "DP" (define pointer) operator is defined to point 1 byte below the target instruction.

Interrupts

Two copies of the SPAD (and condition-code) registers exist, for interrupt and base-level tasks. At reset, the interrupt set are selected. Typically, the initialisation code ends with a JI instruction, which leaves both register-sets' "S" registers pointing at the same instruction. A SET instruction then changes to base level code, which then over-writes the instruction at the JI target with a relative jump to the interrupt routine. This interrupt routine is coded as a loop, which finishes with a SET
base level>. The following instruction will jump back to the head of the interrupt routine.

Hence an interrupt switches register sets, and immediately jumps to the head of the interrupt routine. After interrupt processing is done, the SET
base level> is executed, leaving the interrupt level's S pointing at its successor instruction, ie the jump back to the head of the interrupt routine. Processing then resumes in the base-level registers.

Next issue

This article has described Simplex-III from a programmer's standpoint. The next article will cover the hardware debugging facilities.

```
Table 3
        Branch-Condition Codes
14 15 16
         Condition
0 0 0
         Not zero
         Zero
0 0 1
0 1 0
         Not negative
         Negative
0 1 1
  0 0
         Not carry
1
1
  0
     1
         Carry
  1
     0
         Always
1
         Sense switch ON (on front-panel)
1 1 1
```

```
Table 5 :Typical Subroutine Entry/Exit Sequence

SUBPTR DP SUBROUTINE //Point below 1st byte of code //Calling routine

JIL X2,X3,SUBPTR //SUBPTR accessible from X3 //Link (X2) points to JIL instr. //Caller continues

SUBROUTINE //Subroutine code: link in X2 //Save X2 if reqd.

MIR S,X2,2 //S = X2+2, ie return past JIL

JIL A,X3,SUBPTR //As above, but link is discarded // (no link is ever stored in A)
```

Machine instructions

Definitions:

Ro = The operand register (A, X1, X2, X3) Rx = The index register (S, X1, X2, X3)

= Offset byte from instruction (zero extended to 16 bits)

= The effective memory operand address, defined as (rx + I)

q = Content of Q

Where the target of an operation is shown as "z, c" this means the C (condition) bits are affected, as well as loading a result into z.

The instruction assignments are as follows:

Code 0 1 2 3 4 5	Mnemonic ADD ro + q => ro, c ST ro => q LD q => ro, c XOR ro XOR q => ro, c AND ro AND q => ro, c LCP ro AND q => c	Function //Add memory to register //Sore register //LD sets conditions, unlike the 8086 //Exclusive OR memory to register //Logical AND memory to register //AND, but don't store result
6	ADS ro + q => q, c	//Add register into store
7	SUB ro - q => ro, c	//Subtract memory from register
8	CMP ro - $q => c$	//Subtract, but don't store result
9	JI/JILq => s	//Jump indirect/link. See text for side effects
A	CTS q + 1 => q, c	//Count in store. Always 1-byte operand
В	SET	//Set values for operand length, interrupt terminate, etc.
C	RTL ro + ro => ro, c	//Add to itself, ie shift left
Ď	BC s +/- l => s	//Branch on conditions. Direction, and
	20 0	condition set by Ro, Ri bits
E	LDI I => ro, c	//Load immediate, 8-bit zero-extended
F	MIR $ro + l => rx$, c	//Move/increment register. Effectively moves Ro+I to Rx

Adding the 16550 UART to a 65xx system

by André Fachat

Special Feature
Interfacing

6502 + 16550A

How to add a 16550A UART to a 65xx system

I have stumbled across quite a few 6502 computers that use the 6551 ACIA for a serial interface. When I used this chip, I found it rather slow. Since I was doing a Multitasking operating system for the 6502, the interrupt latency became too large to reliably catch each and every character from the device even at 2400 Baud. This was even worse on the 1MHz my C64, into which I had built an ACIA interface in a socket under the SID 6581 (sound chip).

I had already heard of the 'FIFO-serial interface' for PCs, and even replaced some 8250's with 16550A's myself. So I decided to replace the ACIA in my C64 with the 16550A UART.

Bus differences

The 16550A UART chip was designed for a different bus than the 6502, so there are differences in how to handle the chip. When I had a first look at the interface, I really thought, 'why did they build the chip this way!'.

The Reset line is high active - which places the chip in "running mode" at power up, and then an explicit signal on the Reset line only resets the chip. The 65xx series use an active low -RESET line, such that even a simple RC-element with an additional Schmitt-Trigger suffices for a simple computer.

The Interrupt line is high active also. You can not wire-or it together with other devices (brain-damaged PC design!) as in 65xx systems for example. (That would even work if the passive state would be to leave the line, and not to pull it down to 0 Volts - but that's PC design...) And of course, there is no general clock line, but accesses take place during active RD/WR lines, as long as the chip is selected. The UART has two read (RD and -RD) and write (WR and -WR) lines, where each triggers a data transfer (i.e. not RD and -RD, but RD or -RD — which is IMHO quite peculiar, but I can think of uses for DMA, for example).

These differences in the bus system are, in my opinion, the reason that many people still use the ACIA 6551, and not the much more sophisticated UART 16550A. A more sophisticated chip involves more sophisticated software. In contrary to the simple handling of an ACIA, the UART is indeed more complicated to handle, which also seems a reason for its low usage. In fact there are many caveats in

the UART design that make the thing terrible to program. See the Serial FAQ at ftp://ftp.phil.uni-sb.de/pub/people/chris/The_Serial_Port (and the TCJ FTP site) for more information. But then the UART has the already mentioned advantage of the FIFO, which makes it attractive.

Schematics

When I was rebuilding my ACIA interface to a UART interface, I had to reuse some sockets and chips, because I didn't really want to build everything from scratch (where I didn't have all the parts at home at that time anyway...) The old Interface card was a daugtherboard to be put between the socket for the C64 SID chip and the SID itself. An additional connector gave three signals: A9 to divide the SID address space in half (although the SID has only 28 registers, they are mirrored in a 1kByte block of I/O space in the C64), -E to enable the ACIA at all and -IRQ to signal the CPU. I soldered A9 and -IRQ to appropriate places on the C64 motherboard, while -E goes to a switch.

With the ACIA and the use of a dual 2-to-4 decoder 74LS139, I was able to do the whole thing. It even made the ACIA disappear from the memory map, when it was disabled. This didn't work with the UART, because I needed more circuitry from the decoder to manage the RD/WR handling. Well, one could surely think of something cleaner, but I wanted it quick...

Here's how it works in the C64

All pins from the SID are connected from the C64 SID socket to the SID socket on the daughterboard, except -CS (pin 8). This line is or'ed with the additional A9, to remove the SID from the upper half of its memory window, and then given to the SID. The first half of the '139 then gives the condition that Phi2 is high, -CS is active, and A9 is high. This output is then fed into the -E pin of the second decoder. The enable line (from the external enable switch) switches between the two used and the two not used outputs of the decoder. R/-W as the lower decoder address line then switches between the RD and the WR line. These outputs are or'ed with the inverted Phi2, and fed to the UART.

This arrangements has two purposes: The two decoder stages that have Phi2 in the first decoder give a delay to the beginning of the access. This is needed, as the C64 switches from video chip memory access to CPU memory access with the phases of Phi2. So the address lines need some time to

adjust. (The VIA 6522, for example, expects the address lines valid at the beginning of Phi2, and doesn't work with the C64 that way. It needs the starting transition of Phi2 to be delayed.) The ORing with the inverted Phi2 then stops the access by invalidating the RD/WR lines when Phi2 becomes inactive. This also is a reason for Phi2 being used as CS line.

Another example

I have also built a Dual UART card with two 16550A for my selfbuilt 6502 computer, and there I used a similar approach. I took a 74LS138, a 3-to-8 decoder. The select line for the I/O area goes to the decoder as enable line (-E1), as well as Phi2 (E3). -E2 is not used and set low. A0 is connected to R/-W of the system, and A1 is another address line. A2 is also set low. The outputs Q0-Q3 are then connected to the two chips.

-Q0 -> UART1 -WR -Q1 -> UART1 -RD -Q2 -> UART2 -WR -Q3 -> UART2 -RD

The Software

Now that you have the UART in your computer, you have to have some software to use it. I have not yet rewritten the C64 OS to use the UART as serial interface (which I had done to use the ACIA before). Maybe I have this ready, when this issue of TCJ comes out, then you find it on my homepage http://www.tu-chemnitz.de/~fachat/. But I have already written a generic UART device driver for my selfbuilt 6502 Operating System, OS/A65.

The code shown here is part of that driver, together with a simple C64 binding. It actually follows the suggestions given in the "Serial FAQ". I have one problem, though. Because the interrupt generation is somehow buggy in the UART, the FAQ suggests to start the transmitter from outside the IRQ routine. Well, in my OS I don't have any device code outside the IRQ routine (that is called when data is being sent). But then, as the 6502 cannot directly decide where an IRQ came from, the interrupt drivers are (almost) all called when an IRQ occurs, with "higher priority" first. So the serial driver, being the one with the highest priority, is called very often, even if it is not the source of the IRQ itself. But that ensures that the IRQ routine is called and so I can check there, if I have to start transmission manually.

The listed program echos characters it receives from the serial line back to the serial line. It also takes characters typed on the C64 and sends them to the serial line. A part of the screen is used as character buffer, so that you can see something, when the program receives characters.

I have written a SLIP (Serial Line Internet Protocol) program for my selfwritten OS, that uses an UART. On my 1 MHz C64 with builtin UART it replies to Internet PING messages without packet loss at 9600 baud. Using the same program with an ACIA, even at 2400 baud, is completely useless due to lost characters.

Conclusion

The 16550A might not be the chip of choice for simple applications, where a high data rate is not necessary. But if you don't want to use the serial line as a terminal line only, but want to do some serious data transfer, better take an UART. Here you see a way to use the UART in 6502 based systems and how to program it.

André Fachat (a.fachat@physik.tu-chemnitz.de)

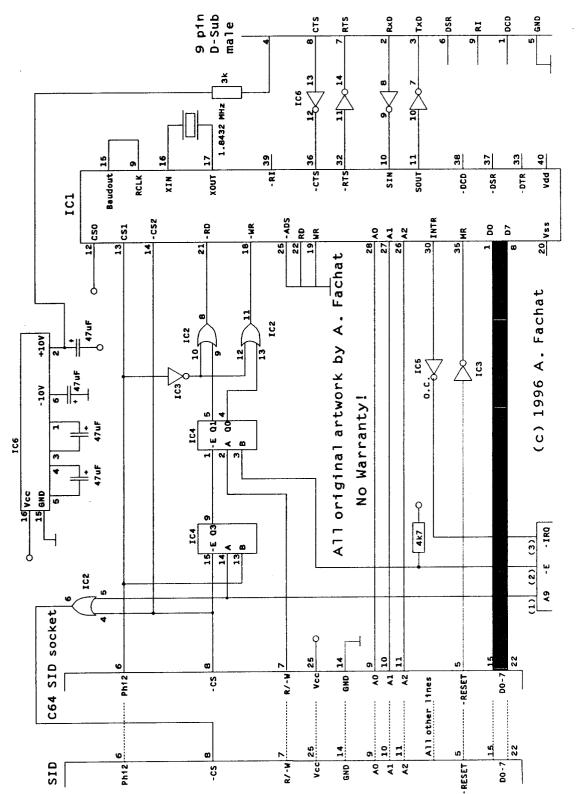
```
(c) 1996-1997 Andre Fachat
    fachat@physik.tu-chemnitz.de
    This is part of a UART 16550A serial line driver for the OS/A65 operating system.
    The 16550 is not really an easy chip, but it has 16 byte input and output FIFO buffers, which allows much higher interrupt latencies.
    routines defined here are:
    devini – initializes 16550A hardware
    devirg - must be called in the interrupt
                            routine
                            sets the speed of the transmission
    setspeed
                             (yr = speed index in the divisor
                             table)
                         - switches transmitting on/off
    txon/txoff

    switches receiving on/off

    rxon/rxoff
    routines needed are:

    read byte from application in IRQ
(via software FIFO)

    GETC
                            write byte to application from IRQ (via software FIFO)
    PUTC
    STRCMD - get status of software FIFO
/* UART register definitions */
                                   /* DIAR=0 */
#define RXTX
                                   /* DLAB=0 */
#define IER
                                  /* divisor low, DLAB=1 */
/* divisor high, DLAB=1 */
#define DLL
                              0
#define DIH
                                  /* Irq ID Reg, read only */
/* FIFO Control, write only */
/* Line Ctrl Reg */
/* Modem Ctrl Reg */
/* Line Status Reg */
#define IIR
#define FCR
#define LCR
#define MCR
#define LSR
#define MSR
                                  /* Modem Status Reg */
/* 'scratchpad', unused */
#define SCR
/* UART is the (memory mapped) address of the UART \star The E_* codes are distinct error codes. E_OK is
     ), the others are not.
'status" is a local va
                  is a local variable */
    status: Bit 0 = 1= handshake enabled
                         1 : l= no ACIA found
5 : l= set RTS hi
6 : l= we are transmitting (DC_SW_TX)
7 : l= we are receiving (DC_SW_RX)
               DC_SW_RX %10000000
DC_SW_TX %01000000
#define
#define
/* 16550 divisor values for BAUD rates ?. 50, 75  
* 110, 134.5, 150, 300, 600, 1200, 1800, 2400,  
* 3600, 4800, 7200, 9600, 19200
               .word -1, 2304, 1536, 1047, 857, 768, 384, .word 192, 96, 64, 48, 32, 24, 16, 12, 6
               .word -1,
divisor
/***************
 * init UART
    This routine is according to the Serial FAQ by Chris Blum, Release 18. The FAQ is posted regularly to comp.sys.ibm.pc.hardware.comm and comp.os.msdos.programmer and can be obtained by ftp at ftp://ftp.phil.uni-sb.de/pub/people/chris/
```



All SID pins connected through from C64 to new SID socket, except pin 8, -CS The usual Power Supply connections apply..

		se IC5 with pullups			
16550A	74LS32	74LS00 (or us	74LS139	7416	MAX232
101	IC2	103	IC4	105	106

```
* The_Serial_Port
  * (These routines get called with the device number * in the x register. As this driver supports one * UART only, x is always 0 - that may change) */
               sta status
;check if there's something like an UART at all
ldy UART+MCR
lda #$10
                 sta UART+MCR
                 lda UART+MSR
                 and #$f0
                 bne nodev
                 lda #$1f
sta UART+MCR
                 1da UART+MSR
                 and #$f0
cmp #$f0
                 bne nodev
sty UART+MCR; check if it has a scratchpad register; if not then it's plain 8250
ldy UART+SCR
lda #$10101010
                sta UART+SCR
cmp UART+SCR
                 bne dev8250
                 lsr
                 sta UART+SCR
                 cmp UART+SCR
bne dev8250
sty UART+SCR
; now check the 16xxx versions
                lda #1
sta UART+FCR
                 lda UART+IIR
                ldy #0
sty UART+FCR
                bcc dev16450
                 asl
bcc dev16550
: else dev16550A; currently only this one
: is supported
  ok, we detected a 16550A, i.e. a chip with working FIFO
lda #%10000000
sta UART+LCR
ldx #14*2 ; 9600 BAUD
                lda divisor,x
                sta UART+DLL
                lda divisor+1.x
sta UART+DLH
                1da #%00000011
                                                    : 8N1
                sta ÜART+LCR
                                         ; no FIFO enable and
                1da #7
                ; clear FIFOs,
sta UART+FCR; trigger at 1 byte
                lda #0
sta UART+IER ; polled mode (so far)
sta UART+MCR ; reset DTR, RTS
              clc
              rts
                             ; no UART at all
nodev
                             no Scratchpad, no FIFO scratchpad, no FIFO FIFO bug
dev8250
dev16450
dev16550
                lda status
                ora #2
                sta status
                1da #E_NOTIMP
                sec
                rts
/************
 * UART interrupt routine
 * The interrupt routines are called one after each * other for every device in this OS.
* If an interrupt source has been removed, then * E_OK is returned, E_NOIRQ otherwise. So this * routine even gets called, when lower level * interrupts occur. This is due to the single level * interrupt structure of the 6502 (not counting the * NMI, which is not really of use in this OS)
```

```
The routine is nasty due to several reasons: The UART doesn't periodically generate interrupts, when the transmitter is empty, as the ACIA does. So it is possible to be able to send (i.e. put characters in software send FIFO) but the interrupt driven driver doesn't know about it.
      interrupt driven driver doesn't know about it. Therefore, the Serial FAQ suggests to start the transmission manually when data is written to the drivers internal buffers. In this OS the buffers (software FIFOs) are totally independent FIFOs (Streams) written to and read with PUTC and GETC. To avoid lockups, I therefore check if I can start sending every time the interrupt routine is called, even if the interrupt source is not the UART itself
        is not the UART itself.
      The FAQ suggests checking if data is to be sent after all UART interrupt sources have been handled. But "Start transmission by simply calling the tx interrupt handler after you've written to the tx fifo [software-FIFO] of the program..." (These are things you can do with DOS.... ts,ts,ts) doesn't work here. Instead we check it in every interrupt call. */
devira
                      Ìda UART+IIR ; UART IIR
                      lsr
                   bcc intr ; ok, found IRQ
lda #E_NOIRQ ; no irq source found
jmp irqe ; not this one
                      bcc intr
irgend
intr
                      and #%00000011
                                                                     ; interrupt mask - makes
                                                    ; four possible IRQs
                      tay
                      bne int_tx
                     ; modem status interrupt
lda UART+MSR ; de-locked by reading the MSR
jmp checkint ; do it, even if this IRQ is
; not enabled...
int_tx
                      dey
                      bne int_rx
                                                     ; transmitter empty interrupt
; write data bytes to UART
; FIFO
tx_loop
                      jsr tx2
                      jmp checkint
int rx
                      dey
                      bne int_status
                                                     ; receiver interrupt
rx_loop
                      jsr rx2
                                                      ; get one char and save
                      ida UART+LSR
                      1sr
                                                   ; still data in UART FIFO?
                     bcs rx_loop
jmp checkint
int status
                      lda UART+LSR ; line status interrupt
                                                     ; de-locked by reading MSR
                                                     ; still another IRQ pending?
checkint
                      lda UART+IIR
                      lsr
                                                    ; irq still pending
; check if we are still
; allowed to rx (i.e. stream
; has not been closed from
                      bcc intr
                      jsr nobyt
                                                      ; reader)
                   lda #E_OK
                                                      ; irq source removed
irqok
                                                         we get here no matter if
UART IRQ or not
check if we are allowed to
start sending manually
(THRE = LSR bit 6)
irge
                     pha
                      1da UART+LSR
                      and #$40
                                                        no then end
otherwise fill FIFO
check if we are still
                     beq nbyt
jsr tx2
                      isr nobyt.
                                                      ; allowed to receive (this ; ensures to check even if no
                                                      ; traffic)
nbvt
                     pla
rts
                          Receive a single byte
rx2
                      lda UART+RXTX: load data byte
```

```
; are we receiving?; no, then end; and save in software FIFO
                                                                                                      sta UART+MCR
             bit status
             bpl rx2end
jsr PUTC
                                                                                                      lda status,x
and #%11011111
              bcc rx2end
cmp #E_SLWM
                                  : no error -> end
                                                                                                      sta status,x
                                  ; stream below low water mark? ; this happens most and is
                                                                                                      rts
              bne test
                                                                                        ; caught by nobyt anyway
                                                                                         * control handling
rx2end
             rts
                                                                                         * This is rather OS specific, so maybe it's not
* necessary here. One thing to mention is, that
* rxoff and txoff just reset their bit in the status
* byte. rxoff then sets RTS high (rtsoff). After
* that, both check if transmitter or receiver are on.
* If both are shut off, then DTR is set high
              ; check stream (software-FIFO) status
&nobyt
                                  ; are we receiving?
; no -> end
; get state of stream
; ok -> end
             bit status
             bpl rx2end
jsr STRCMD
             bcc rx2end
                                                                                            (dtroff).
test
                                  ; stream has been closed from
             cmp #E_NUL
                                                                                         * If the transmitter or receiver are enabled, both * set DTR low (dtron). The receiver also sets CTS \,
                                  ; reader?
             bne tstwater
                                                                                          * low (ctslo).
              jmp rxoff
                                  ; yes, then shut receiver off
tstwater
              cmp #E_SEMPTY; stream is empty?
              beq wi
                                  ; ok, ensure that RTS is low
                                                                                        rxon
                                                                                                      jsr rtson
                                                                                                      jsr dtron
lda #DC_SW_RX
              tax
                                  ; we want RTS hi?
              lda status
                                                                                                      bne o2a
              and #1
                                  ; yes, then high
             bne wh
                                                                                                      jsr dtron
lda #DC_SW_TX
ora status
sta status
                                                                                        txon
              txa
             cmp #E_SFULL ; stream full
beq wh : then RTS high
cmp #E_SHWM ; stream above high water
                                                                                        o2a
                                                                                                      bne ok
                                  ; mark?
                                           ; no then branch
             bne twl
              1dx #0
                                                                                        rxaff
                                                                                                      lda status and #DC_SW_RX
wh
              jmp rtsoff
             cmp #E_SLWM : stream below low water mark? bne rx2end : no then end ldx #0: otherwise RTS low jmp rtson
                                                                                                     beq devoff
jsr rtsoff
eof to software FIFO here
twl
                                                                                        ; signal
wl
                                                                                                      lda status and #255-DC_SW_RX
                                                                                                      sta status
              ; Fill transmitter FIFO
                                                                                                      jmp checkdtr
tx2
             bit status ; are we transmitting?
bvc txrt ; reading IIR should clear
; this line
lda UART+MSR ; are CTS and DSR ok?
                                                                                                      lda status and #DC_SN_TX
                                                                                        txoff
                                                                                                      beg devoff
                                                                                        ; signal
                                                                                                     close to software FIFO here
             and #%00110000
cmp #%00110000
bne txrt ;
                                                                                                      lda status
and #255-DC_SW_TX
                                            ; cts or dsr inactive
                                 ; yes then end
                                                                                                      sta status,x
             ldy #15
                                           ; number of byte
                                                                                        checkdtr and #DC_SW_TX+DC_SW_RX
txloop
                                                                                                      bne active
jsr dtroff
              jsr GETC
             bcs test2
             sta UART+RXTX; send new data byte
                                                                                        active
                                                                                                      jmp ok
             dey
bne txloop
                                 ; fill up FIFO
                                                                                        setspeed tya
                                                                                                      and #%00001111
             bcc txrt
cmp #E_EOF
bne txrt
                                  ; we got a stream End-Of-File?
                                                                                                      asl
test2
                                                                                                      tax
             jmp txoff
                                  ; yes, then shut transmitter : off
                                                                                                      beg ok
1da UART+LCR
                                                                                                      ora #$80
sta UART+LCR
txrt
             rts
             .)
                                                                                                      lda divisor.x
sta UART+DLL
lda divisor+1.x
sta UART+DLH
 * support routines */
             lda UART+MCR
and #%11111110
sta UART+MCR
lda #0
sta UART+IER
                                                                                                      1da UART+LCR and #$7f
dtroff
                                                                                                      sta UART+LCR
                                                                                                      lda #E_OK
                                                                                                      .byt $2c
lda #E_DON
             rts
                                                                                        devon
                                                                                                      .byt $2c
lda #E_DOFF
             lda UART+MCR
ora #%00000001
sta UART+MCR
lda #3
sta UART+IER
dtron
                                                                                        devoff
                                                                                                       byt $2c
                                                                                                     lda #E_NOTIMP
cmp #1
                                                                                        onotimp
                                                                                                      rts
             lda UART+MCR
and #%11111101
sta UART+MCR
rtsoff
             lda status.x
ora #%00100000
             sta status,x
             rts
             1da UART+MCR
ora #%00000010
rtson
```

Regular Feature All Users

dBase II & TCAP

The European Beat

by Helmut Jungkunz

Z-BASE - A way to use ZCPR's TCAP for dBASE II

When CP/M is mentioned, one often hears or reads the term "standard program". The most popular so-called standard programs then were WordStar, Multiplan and dBASE. I always liked dBASE, for it offered even blunt idiots like me an easy interface to screen-oriented programming, even if in very rudimentary form.

What annoyed me, was the fact, that dBASE had to be installed for each and every terminal. When ZCPR came about, I first thought:

Wow - finally no more installations of terminals! Well, that goes for ZCPR - aware programs and tools only. When you use dBASE or any other non-ZCPR-program, you would still have to install the program first.

One of the nice things in UNIX and in ZCPR is the use of a so-called TCAP (Terminal CAPabilities) file, that, once loaded, will provide a given screen environment, usable by all applications for that system.

dBASE by itself does not offer any possibilities to directly make use of the ZCPR TCAP, but it has a powerful, built-in interface to PEEK and POKE memory addresses and thus to execute machine code!

The theory of all that may be taken from the program in BOX 1.

"CALL <memory variable>" will branch processing to the address specified in a SET CALL TO <address> command. The address must be decimal. When you reach the called address, the register pair H-L points to the first byte of the memory variable; this

```
BOX [ 1 ] "DBASPOKE.INF".
Technical Support Note # 25
Copyright 1983, Ashton-Tate, All Rights Reserved
General Distribution
                                                                            28 Mar 1983
Assembly code interface information for dBASE II 2.3B running on CP/M 2.2 .
The syntax for PEEK, POKE, and CALL is as follows:
PEEK( <address> )
POKE <address>, <byte list>
SET CALL TO <address>
CALL (memory variable)
          POKE stores a list of values into a specified location in the r's memory. PEEK is a numeric function that returns the value
computer's memory.
of a specified byte in the computer's memory. Both PEEK and POKE use
decimal addresses and values.
Examples:
STORE PEEK(128) TO value
STORE 128 TO location
? PEEK(location), PEEK(location+1)
* Subroutine..: LEADZERO.LIB
* Description.: Replaces leading blanks with leading zeroes.
POKE 42000, 34, 37,164, 70, 35,126,254, 32

POKE 42008, 194, 33,164, 54, 48, 5,194, 20

POKE 42016, 164, 42, 37,164,201

STORE " 123" TO number
CALL number
? number
  LEADZERO.ASM Replacing leading blanks with leading zeroes.
; Written by Luis A. Castro, Ashton-Tate, 1982.
ÓRG
                      ;Load in dBASE free area.
                      :Save HL registers
SHLD
           SAVEHL
                                 ;Store length of string to counter.
                                 ;Skip to next character
LOOP:
           MOV
                      M,A
                                 ;Fetch character
           CPI
                                 ; Is it a space?
           JNZ
                      DONE
                                 ;Yes, done.
                      M,'0'
                                 Replace space with zero
           ΙVΜ
                                 Decrement counter
           DCR
                      LOOP
                                 Repeat until done
           JNZ
                                 Restore HL registers.
DONE:
           LHLD
                      SAVEHL
           RET
SAVEHL DS
   Program.: HEX-DEC.CMD
  Author..: Luis A. Castro.
Date...: 9/14/82, 7/12/83.
Notice..: Copyright 1982, ASHTON-TATE.
Notes..: To convert an assembled program's HEX file into a dBASE POKE sequence. This program works only
      with HEX dumps that look like the following:
             :10A410002225A446237EFE20C221A4363005C21484
             :05A42000A42A25A4C9D7
             :0000000000
```

```
The file this program generates is a .LIB file and can be added to a dBASE command file using an editor \,
  *
          or word-processor.
          You will need to create HEX-DEC.DBF with the structure:
                   HDUMMY1
  *
                                                   001
                   HLENGTH
                                                   002
                   HADDRESS
                                                   004
  *
                   HDUMMY 2
                                                   002
                                        002
                  H11
                                                   002
                  H12
                                                   002
                  H13
  *
                                                   002
                  H14
                                                   002
                  H15
  *
                                                   002
                  H16
                                                   002
                  H17
  *
                                                   002
                  H18
                                                   002
                  H19
  *
                                                   002
                  H20
                                                   002
                  H21
                                                   002
                  H22
                                                   002
                  H23
                                                   002
                  H24
                                                   002
                  H25
                                                   002
                  H26
  SET TALK OFF
STORE "123456789ABCDEF" TO hexvalues
 * Macros to convert hex values to decimal values.

* Macros to convert hex values to decimal values.

* Macros to convert hex values to decimal values.

* Macros to convert hex values to decimal values.

* Macros to convert hex values.

* O($(Hlength, 2, 1), hexvalues)] TO Mhexlen

* STORE [@($(Haddress, 1, 1), hexvalues)*4096 +;

* O($(Haddress, 2, 1), hexvalues)*256 + O($(Haddress, 3, 1), hexvalues)*16 +;

* O($(Haddress, 4, 1), hexvalues)] TO Mhexaddr
  ERASE
? "CONVERTING A HEX DUMP TO DECIMAL"
  .
ACCEPT "Enter hex file...." TO filename
IF_filename=" "
  RETURN
  ENDIF
  IF @(".",filename) > 0
STORE $(filename,1,@(".",filename)-1) TO filename
  ENDIF
  STORE !(filename)+".HEX" TO infile
STORE !(filename)+".LIB" TO outfile
ACCEPT "Enter description.." TO notes
  ? "Copying structure to HEX-DEC...."
 USE Hex-dec
COPY STRUCTURE TO Hex-dec.$$$
 USE Hex-dec.$$$
? "Appending from &infile....."
APPEND FROM &infile SDF
GO TOP
ERASE

SET ALTERNATE TO &outfile

SET ALTERNATE ON
? [* Subroutine..: ]+outfile
? [* Description.: ]+notes
STORE &Mhexaddr TO address
? [SET CALL TO ]+STR(address,5)
? [* 0 1 2 3
[ 11 12 13 14 15]
DO WHILE "13
                                                                                                                 9 10]+;
                                                                               5
                                                                                       6
                                                                                                7
                                                                                                        8
  [ 11 12 13 14
DO WHILE .NOT. EOF
  STORE &Mhexlen TO linelen
STORE &Mhexaddr TO address
 If linelen <> 0
STORE "" TO decimals
STORE "11" TO item
DO WHILE VAL(item)-10 <= linelen
STORE decimals+","+STR(@($(H&item,1,1),hexvalues)*16;
+ @($(H&item,2,1),hexvalues),3) TO decimals
STORE STR(VAL(item)+1,2) TO item
FNDDO
  ENDDO
  ?"[POKE ]+STR(address,5)+[,]+$(decimals,3,LEN(decimals)-2)ENDIF
  ENDDO while .not. eof
SET ALTERNATE OFF
  DELETE FILE Hex-dec.$$$
  QUIT
  * EOF hex-dec.cmd
```

is the length byte for character strings. The <memory variable> must be a string and may not be lengthened while you are putting data into it. Execute a machine language return to get back to dBASE. dBASE will handle saving the registers. All machine memory from A400H up to the bottom of the CP/M BDOS is available, but will be overwritten when a SORT is done. It is recommended that a MOVCPM utility be used to create protected memory areas for assembly routines above CP/M.

To convert an assembled program's hex file into a dBASE POKE sequence you may want to run the dBASE program HEX-DEC.CMD provided for you at the end of this documentation.

This was released some time ago over the internet and tells the story. I now sat down and took a look at the ZCPR environment. Each TCAP sits in memory, once ZCPR has started. Considering the latest TCAP version, the address of the graphic characters used by the terminals (GOELD) is at a defined offset of 13 from the start of "TCAP". "TCAP" is found at the page just above the Z3 environment address ENV.

To find these addresses, issue from NZCOM or Z3PLUS the command ENV. This macro will peek the corresponding page of Z3ENV for your system. Take down the hexadecimal address at the left top! That is all you need (plus the tool ZDDTZ.COM or a Hex-Calculator). In my case, I have the address F580 for ENV. I start ZDDTZ and enter:

```
DDTZ v2.5 by C.B. Falconer.
CPU=Z80
-hF580 (the - is the prompt, the rest is entered from the keyboard)
F580 62848 (This is what we want - the decimal form of the address!)
^C
A:>
(done)
```

Now we take down 62848 on a piece of paper. We use ZDE to edit our dBASE "TCAP.CMD" and enter this decimal address as the value for ENV. Everything else is calculated automatically.

Now bring up dBASE and issue the command:

DO TCAP

The screen will be erased and after a while, GOELD will appear at the top of your Monitor, followed by a colon ":". This is called by a fake "Strikeany-key-when-ready" command ->

accept to dummy

You may leave this out, but for debugging purposes, I think it is a great help. Once you strike your "ANY" key (okay, bad joke), the graphical characters from your extended TCAP will be displayed.

If you have an idea, how the HEX-TO-DEC routine shown here can be used to immediately return the ENV address in decimal to dBASE, I would certainly appreciate this.

Just to be complete, I also include a dummy extended TCAP, that can be used on all non-graphical terminals to use standard characters like "+","-","!" and so on.

This is an example, of how a Televideo terminal with no graphical characters may be turned into a "Graphical Terminal". This is a legal hoax that works nicely to convince ZCPR, your terminal can do it. And as a matter of fact. it does.

Regards from Germany

Helmut Jungkunz helmut.jungkunz@metronet.de

```
BOX [ 2 ]
                 TCAP.CMD
*Routine TCAP.CMD by Helmut Jungkunz, ZNODE 51, Germany
erase
*thex TO dec CONVERSION routine NEEDED
* Here I enter the address of my Z3ENV in decimal manually * to get this address, issue the command ENV from NZCOM or Z3PLUS
store 62848 to ENV
store (ENV+128) to ENV
store (ENV+13) to GOELD
? "GOELD =",GOELD
*the nect line is a "wait for any key pressed ..."
accept to dummy
store GOELD+17 to count
store count+16+peek(count) to count
store chr(peek(count)) to UL
*UL is Upper Left of a box
? count.UL
store (count+1) to count
store chr(peek(count)) to UR
*UR is Upper Right of a box
? count,UR
store (count+1) to count
store chr(peek(count)) to LL
*LL is Lower Left of a box
? count.LL
store (count+1) to count
store chr(peek(count)) to LR
*LR is Lower Right of a box
? count.LR
store (count+1) to count
store chr(peek(count)) to HL
*HL is Horizontal Line of a box
? count,HL
store (count+1) to count
store chr(peek(count)) to VL
*VL is Vertical Line of a box
? count.VL
store (count+1) to count
store chr(peek(count)) to FB
*FB is the character Full Block
? count,FB
store (count+1) to count
store chr(peek(count)) to HB
*HB is the character Half Block
? count, HB
store (count+1) to count
store chr(peek(count)) to TI
*TI is the character Top Intersection
? count,TI
store (count+1) to count
store chr(peek(count)) to BI
*BI is the character Bottom Intersection
? count.BI
store (count+1) to count
store chr(peek(count)) to MI
*MI is the character Middle Intersection
? count,MI
store (count+1) to count
store chr(peek(count)) to RI
*RI is the character Right Intersection
? count,RI
store (count+1) to count
store chr(peek(count)) to LI
*LI is the character Left Intersection
? count,LI
store (count+1) to count
enddo
             end of TCAP.CMD -
BOX [ 3 ] DUMBTERM.Z80
  Z3TCAP file: Z3TCAP.Z80
         EQU 27
                             ; Escape character
  The first character in the terminal name must not be a space. For
: Z3TCAP.TCP library purposes only, the name terminates with a space ; and must be unique in the first eight characters.
TNAME: DB
                                           ; Name of terminal (13 chars)
GOFF:
                GOELD-TNAME ; Graphics offset from Z3TCAP start
```

; Terminal configuration bytes B14 and B15 are defined and bits assigned as follows. The remaining bits are not current Set these bits according to your terminal configuration.

The Computer Journal / #80

The remaining bits are not currently assigned.

```
B14 b7: Z3TCAP Type.... 0 = Standard TCAP 1 = Extended TCAP
             bit: 76543210
B14:
            DB 10000000B; Configuration byte B14
            B15 b0: Standout..... 0 = Half-Intens
B15 b1: Power Up Delay. 0 = None
B15 b2: No Auto Wrap... 0 = Auto Wrap
B15 b3: No Auto Scroll. 0 = Auto Scroll
                                                ... 0 = Half-Intensity 1 = Reverse Video
                                                                                      1 = Ten-second delay

1 = No Auto Wrap

1 = No Auto Scroll
             B15 b4: ANSI..... 0 = ASCII
            bit: 76543210
DB 00000000B; Configuration byte B15
B15:
  Single character arrow keys or WordStar diamond
B 'K'-40H ; Cursor up
B 'V'-40H ; Cursor down
B 'L'-40H ; Cursor right
                                      Cursor up
Cursor down
Cursor right
Cursor left
ĎΒ
DB
DB
             'H' - 40H
DR
; Delays (in ms) after sending terminal control
 strings
                                ; CL delay
; CM delay
ŃΒ
DB
             n
                                : CE delay
DB
  Strings start here
L: DB 'Z'-40H.0 ; Home cursor and clear screen
M: DB ESC,'=%+ %+ '.0 ; Cursor motion macro
E: DB ESC,'T'.0 ; Erase from cursor to end-of-line
0: DB ESC,'G4',0 ; Start standout mode
E: DB ESC,'G0',0 ; End standout mode
I: DB ESC,'G0',0 ; Terminal initialization
E: DB ESC,'G0',0 ; Terminal deinitialization
; S
CL:
CM:
CE:
SO:
SE:
TI:
TE:
  Extensions to standard Z3TCAP
D: DB ESC, R',O : D
I: DB ESC, E',O : I
D: DB ESC, Y',O : E
                                                 Delete line at cursor position; Insert line at cursor position
ĹD:
LI:
                                                 : Erase from cursor to end-of-screen
CD:
The attribute string contains the four command characters to set the following four attributes for this terminal in the following order: Normal, Blink, Reverse, Underscore
ŚA:
AT:
                                                 ; Set screen attributes macro
             DR
                                                 ; Attribute string
             ĎB
                     0
RC:
                                                 : Read current cursor position
             DB
                     ESC,'?',0
                                                 : Read line until cursor
RL:
: Graphics TCAP area
GOELD: DB
                                      ; Graphics On/Off delay in ms
; Graphics strings
                    '','H'-40H,0
'','H'-40H,0
ESC,'.0',0
ESC,'.3',0
                                                ; Graphics mode On
ĞO:
             DR
                                               Graphics mode Off
Cursor Off
            DB
DB
GE:
CDO:
             ĎB
                                                 : Cursor On
CDE:
 ; Graphics characters
                                      ; Upper left corner
; Upper right corner
; Lower left corner
; Lower right corner
GULC:
            DB
ĞÜRÇ:
             ĎΒ
GLLC:
             DB
                      ٠+،
GLRC:
             DB
                                      ; Horizontal line
; Vertical line
GHL:
             ĎB
GVL:
             ĎΒ
                                       ; Full block
             DB
GFB:
GHB:
                      ٠#٠
                                       ; Hashed block
             ĎΒ
                                      : Upper intersect
: Lower intersect
             ĎB
GUI:
GLI:
             ĎΒ
                                      : Mid intersect
: Right intersect
             DB
GRTI:
             ĎΒ
             ĎB
                                       : Left intersect
GLTI:
 ; Fill remaining space with zeros
  REPT
            128-($-TNAME)
DR
  ËNDM
             END
   End of Z3TCAP
```

Regular Feature

Small System Support

68xx/68xxx Support

C & Assembly

by Ronald W. Anderson

C Class Notes 8, Address Program in C

This time let's digest a typical short program in C and see just how it works. The program reads a data file of names and addresses (and other information if desired) and prints each record that contains a string that matches the string given on the command line. It ignores case. If I give it the command:

address jones

It will print all the records containing "jones" or "Jones" or any combination of caps and lower case. It doesn't just print the line but the whole record. The data file is simply a text file that can be edited with any editor. Records are entered just as they will appear in the printout:

```
* John Jones 1234 5th st. Elko NV 78901
Phone: (000) 111-2222 *
```

The program will list any record that has a match to the search string on the command line. For example it would match the above record to "elk" or "nv". Let's look at the program and then go over it line by line. This program has been left in the style of ANSI C with function prototypes and function arguments defined in this new style.

```
/* address program in C - uses data file of name
    addresses with records separated by lines with asterisk in the first column. Matches a search string and prints each record that
contains the string. */
#include <stdio.h>
#define TRUE 1
#define FALSE 0
// function prototypes
  int read_record(void);
  int match(char *matchbuf);
     int ch;
    char recbuf[600];
FILE *infile;
void main(int argc,char **argv) {
     if (argc ==1)
      puts("address needs a string to match");
     if ((infile = fopen("c:\\addr.dat","r"))== NULL)
          puts("can't open address data file\n");
           exit(1);
// the next line is the main loop of the program.
// It calls the two functions in turn, uses the
    results to produce an output and loops until the end of the data file
     while (read_record()) if (match(argv[1]))
     puts(recbuf);
```

```
fclose(infile);
exit(0);
// this function gets a record in recbuf and
// returns TRUE until end of file is detected at
// which point it returns FALSE.
int read_record(void) {
   int k=0;
   while ((ch =getc(infile)) != '*')
       if (ch == EOF) return FALSE;
       recbuf[k++]=ch;
   recbuf[k] =0;
   return TRUE;
// this function searches recbuf for a match to the
// search string and returns TRUE if it finds one,
// otherwise returns FALSE
int match(char *matchbuf) {
   int m=0,r=0;
   while (recbuf[r])
      while (tolower(recbuf[r++]) ==
                         tolower(matchbuf[m++]))
      if (matchbuf[m] == 0x0ò) return TRUÉ;
      m ≖Ò:
   return FALSE;
```

You might think this is a very short program for what it does. It makes rather full use of the shortcuts available in C. It combines asignment statements and function calls. It uses function call returned values in tests.

You might note that the data file path and name are hard coded into the program, so you must use the filename addr.dat and it must be in your c:\ directory (i.e. the root directory). You can hard code a different name or path if you wish.

Note that we put the main() function first. This is more in line with standard C programming practice. The gurus all say that main is really an outline of your program calling out the various functions in order, and if you are to do top down programming, you should start there. You can block out the called functions to be empty, i.e.:

```
void function() { }
```

Now you can write the functions one at a time and test them, perhaps with a lot of print statements in the function or in main() to test the operation of the function.

While all this sounds good on paper, speaking from expe-

rience, I can say that main() by the time I am done, doesn't resemble main() that I started with! As I look at each function I get ideas for improvements and main() changes accordingly. That doesn't, however, make the approach wrong or invalid. It is always a good idea to block out a program before working on the details. Advocates of top down programming would simply say that I don't spend enough time in the planning stage. I start coding too soon. I would counter that I could spend a very long time planning and my code still would require debug.

I sometimes violate this rule if I know that one function in the program is going to be particularly difficult. I might try to do that one first, doing only a dummy main program that calls it and allows testing of it. Later when the hardest part has been debugged, I'll go back and finish main and then fill in the other, hopefully easier functions.

Well, this has not been a complete item by item discussion of C, but over the last year and a quarter, we have covered the main features of the C programming language. Hopefully at least, this has been done in a way that will allow you to continue with a good textbook on C to learn more.

Whether you have a very small C, one of the dialects of the original Small C, or something more complete like Borland Turbo C or Microsoft Quick C, you will find the differences small. The Small C versions don't have float or double data types, but you can do all of the things we've done in this series. That is, you can manipulate files and do integer arithmetic quite nicely. If you are running a 6809 with FLEX you might be able to find a copy of Windrush C by James McCosh. It has float and double data types and it is not super complicated or large out of line with the resources of a 6809. If you find a later version it will include my scientific function package that I wrote for it and gave to James. If you get an earlier version and want the "scipack" package, let me know and I'll send it to you. I have new and improved sci function algorithms done since then.

If you are an old time reader of '68' Micro Journal you might remember a product called "Duggers Growing C". I was asked to review it way back when, and I found bugs by the dozen. I had access to the source code (in 6809 assembler) of the runtime library and was able to fix a number of bugs, but I couldn't review the thing and give it a "thumbs up", nor could I fix bugs in the compiler proper, since I didn't have source code. I am not talking about bugs in that the compiler didn't meet the then standard (actually one didn't exist then), but just plain operational errors, particularly in the math package.

At the time I offered indirectly to fix it for Duggers. I talked to them and they said "Well, we wrote, compiled and ran a few programs and they ran fine". I guess if that was the extent of their testing, I don't wonder why it was buggy. They did some dumb things, for example testing a 16 bit integer for zero by summing the two 8 bit parts of it. Any value whose upper and lower bytes were 2's complements, like for example, 00000001 11111111 (byte values decimal 1 and -1 in signed arithmetic) when added would produce 8 zeros plus a carry and the carry was ignored so this number and a lot of others tested true for zero! Of course the bytes should have been ORed so that a 1 in any position

would show up in the result and test non zero. I spent a month of evenings fixing numerous such errors and sent Duggers my result. I received a phone call thanking me for my efforts on the runtime package. Though I offered to work on the compiler proper for a copy of the source code, my offer was turned down and the ad was dropped from '68'.

If you have questions, feel free to write. I am still by no means an expert in C, but I can find answers to most questions and would be happy to do so. In the past few weeks I've helped three other programmers with answers to questions about C. I think I am past the beginner stage at last.

Assembler

Let's look this time at some of the more interesting instructions in the 6809 set. For starters how about the MUL instruction. It multiplies the value in the A accumulator by the value in the B accumulator yielding the product in the D accumulator.

LDA #5 LDB #6

The D accumulator now contains: 0000000000011110 This is of course the value 30. If you know that the result is not going to be larger than 8 bits you can consider the answer to be in the B accumulator, i.e. just the 00011110 part of the above. The problem with a multiply is that the result can be so large as to require twice as many bits to represent it.

The beauty of this instruction is that it takes 12 clock cycles and is much faster than the add and shift method that would have to be used otherwise to multiply two 8 bit integers. It is left to the user / programmer how to interpret the result. Assuming unsigned bytes works best or at least is easiest to keep track of. You can assume integer multiply in which case the binary point is at the right end of the result, or you can assume fractional multiply in which case the result must be shifted left one place and the binary point is at the left end of the result. You can handle signed arithmetic by negating negative numbers and keeping track of the sign, re-negating the result if the sign is calculated to be negative. It is a pain for all but the simplest uses, but it can be useful. For example a compiler writer might use it to calculate the offset to the location of a byte or integer in a two dimensional array as the starting location plus the product of the two array subscripts (times 2 for an array of 16 bit integers). It is my belief that some of the less common instructions in the 6809 set were included for writers of compilers to use.

I might mention here that the 68000 instruction set includes both an integer and a fractional multiply called IMUL and FMUL to handle some of the above details for you. It also includes a DIV instruction which the 6809 does not.

I thought it strange when I first saw the 6809 instruction set that it didn't have more instructions that would work on the D accumulator. It has complement and shift instructions

for A and B but not for D. For your thought I offer some subroutines to do some of these instructions.

```
COMD
        COMB
        RTS
NEGD
        COMB
        COMA
        ADDD #1
        RTS
              ;This is a way of giving a subroutine
ASLD EQU
               two names
LSLD
        ASLB
        ROLA
        RTS
ASRD
        ASRA
        RORB
        RTS
LSRD
        LSRA
        RORB
        RTS
```

We probably haven't discussed the difference between Arithmetic shifts and Logical shifts. There is no difference when the shift is to the left. A Zero is shifted into the low order bit.

```
LDA #1
ASLA
or LSLA
result: 00000010
```

The 1 has shifted one place to the left.

Shifting to the right is different, however. The reason is signed arithmetic. When a register contains a signed value, the leftmost bit is the sign bit. When a negative number is divided by 2 the sign bit must be preserved, thus:

```
1111110 (-2)
shifted right one place (ASR)
11111111 (-1)
```

The value has correctly been divided by 2. If we didn't preserve the sign bit as in the LSR instruction, the shifted value would be:

```
01111111 or 127
```

If we are dealing with signed numbers we need to use the ASR instruction but if we are dealing with something like a bit mask we probably want to use the LSR. For example, here is a code fragment to find the highest bit that is a 1 in a byte value:

```
FIND CLRA LOOP CMPB #0
BEQ DONE2
LSRB
INCA
BRA LOOP
DONE2 DECA
RTS
```

A call to FIND would be:

```
LDB VALUE
BSR FIND
```

On return, A contains the number of the highest order bit that was a 1. Bits are counted right to left, the lowest order bit being bit 0 and the highest being bit 7. The algorithm is to shift the value until the remaining value is zero, when

all the bits have been shifted away, counting the shifts. If the VALUE happened to be 0 we get -1 back indicating an error. If the value is 1 A is incremented to 1 for the single required shift but the DECA instruction makes it 0 again which is correct because the low order bit (bit 0) was the only one on. Though this might look like a contrived example, I assure you I have done things like this in the past.

Saving and Restoring Registers

There is a trap you can get into very easily using assembler. Suppose you are going along in some code and have values in both accumulators but you want to go to a subroutine and do something else. If the subroutine needs to use the accumulators to do its thing, the values in A and B that you had in your main program will be lost.

Most of us write subroutines so they save the values from whichever registers they are going to use, and restore these values on exit. The easiest way to do this is to use the system stack and the PSHS and PULS instructions. Subroutine:

```
NAME PSHS A,B
...
instructions using A and B
...
PULS A,B
RTS
```

Of course if you do this you can't return values in A or B (or D). You must return results in a variable somewhere or perhaps in the X or Y registers.

The use of PSHS and PULS instructions requires some great care. Remember that the return address for the subroutine is on the stack. If you Push more bytes than you pull or vice versa, the return address will be corrupted and the program will go off into the wild blue and lock up or start executing garbage!

These are some of the hardest bugs to find and some of the easiest to introduce in a program. Not saving and restoring the contents of a register that needs to be saved is also a hard bug to find in an assembler program.

Had you not guessed, PSHS and PULS instructions are followed by a register list. You can save one register or all of them. The order of the list is unimportant. The processor handles the order so they don't get scrambled by the process.

Of course with multiple instructions you can reverse the order and effectively swap the contents of two registers:

```
PSHS A
PSHS B
PULS A
PULS B
```

This will SWAP the contents of A and B. You must PULL the last thing you PUSHed first. If you DON'T want to swap you must do it this way:

PSHS A PSHS B PULS B PULS A

If you just want to swap two registers the EXG instruction can do that:

EXG A,B EXG X,Y

If you want to copy the contents of A to B or X to Y you use the TFR instruction:

TFR X,Y

This leaves the contents of the first (source) register intact and copies it into the second (destination) register. Note that for either of these instructions the registers to be exchanged or those involved in the TFR must be the same size. You cant EXG A,X. The assembler will flag this error for you.

We ought to discuss the logical AND and OR instructions. First let me say that the operations such as ADD, SUB, AND, OR, EOR etc. all leave the results in the register that is being used.

LDA #5 ANDA #\$FE five = 00000101 \$FE = 11111110 RESULT = 00000100

The AND result is left in A after the execution. The effect of an AND is to turn individual bits OFF. Since our "MASK" had the low order bit off, the result would be to make the contents of A an EVEN number because we have turned the 1's bit off.

LDA #15 ORA #\$10 15 = 00001111 \$10 = 00010000 RESULT= 00011111

The effect of the "MASK" in the case of the OR is to turn individual bits ON.

The AND instruction can be used to see if the contents of A or B have a particular bit ON:

MASK EQU \$04 00000100 LDA VALUE ANDA MASK BNE ...

Whatever VALUE happens to be, the branch will be taken if bit 2 is a 1 and will not be taken if bit 2 is a 0.

There is a test that doesn't destroy the contents of the accumulator. It is the BIT instruction

Suppose in the above example VALUE = 7 After the AND instruction A would contain 4 because we have ANDed away the other bits.

LDA VALUE BITA MASK BNE ...

The result is the same as in the previous case where we used AND, EXCEPT that A now still contains the original value of 7.

The effect of the BIT insruction is to AND the MASK or whatever with the contents of A but NOT to write the result into A. We could do multiple tests in a sequence without having to reload A with VALUE again:

LDA VALUE BITA #\$80 BNE SEVEN BITA #\$40 BNE SIX ...

We could test each bit with a different value to find the highest order bit that is on, as in one of the examples above. This obviously is the hard way to test all 8 bits of a byte value, but if we only wanted to test two or three, it might be fast and short.

There is a similarity in the situation of the SUB and The CMP instructions. We could test for A containing the value 17 a couple of different ways

```
LDA VALUE (assume 17)
SUBA #17
BEQ ...
```

We would branch if the value is 17 because the subtract would make the contents of A zero. The condition code register zero bit would be set. The BEQ instruction looks for the zero bit to decide whether the EQUAL condition is true.

LDA VALUE CMPA #17 BEQ ...

This does exactly the same thing. The CMP instruction subtracts the immediate value and the BEQ test checks the zero bit of the CCR, which is set as the result of the CMP. The difference is that the value in A remains 17. That is, the result of the subtraction is not written back into A.

General

I've recently been given an almost antique 286/12 computer to play with. A friend of mine wanted to upgrade his computer that was considered quite a machine in 1988 when he bought it. It has a 360K 5.25 inch floppy drive, a 1.44 Mbyte 3.5", 640K of memory, a 145 watt power supply, a 40 Mbyte hard drive (IDE), and a reasonably nice AT style keyboard. It also had an EGA display board.

We decided after a good look that about the only parts of any value for an upgrade would be the keyboard and the 1.44 Mbyte floppy drive. He decided he might as well buy a new one and told me to keep it with an eye toward giving it to someone or some organization who might be able to use it. Yes, things surely do get obsolete quickly. The sad part is that the computer runs fine. With the addition of an old VGA board, and by plugging my monitor and mouse onto it, I checked it all out and loaded some software on it. It works flawlessly except that it is about 15 times slower than my present 486 system. If I needed only a fairly simple word processor system, I could have one very inexpensively with a computer like this as a start. Actually it would work admirably for what I am doing right now, using it as a

simple word processor to write this column. If I wanted more storage, I would probably only add a larger hard drive and some more memory. The motherboard has four simm sockets so it looks as though I could add up to 4 Mbytes, though there is no documentation and it might be a problem to get it all running again.

My present system is most likely 2 to 3 times slower than the new pentium systems hitting the market currently. I've always been happy with a computer until I've used a faster one for a short while. The old 6809 system used to be great fun to use. Now when I compile a program and have to wait five minutes, I writhe in the pain of boredom. I can compile the equivalent program on my latest computer in a few seconds.

When I started using 68000 based systems with real MFM hard drives, I was in heaven. Those 5 or 10 minute compiles could be done in 2 or 3 minutes. Hard disk data transfer, while vastly faster than with floppy drives, was still a bit slow.

The 286 based system I bought (12 MHz) seemed to be a whiz until I got my hands on a 386-40. Then came the 486 system. Each time, as I said, a few days use of the newer and faster system made the old one seem like it had been filled with molasses! Actually, my 486SLC50/2 is built on a motherboard that will accept and run a 66/2 as well. The clock frequency is changed by moving one jumper. Just for fun I decided to try running the processor (clearly marked as a 50 MHz one) at 66. It worked fine. Someone at work reminded me that the 66 version of this board has a heat sink on the processor chip. I switched back to 50 temporarily and went and bought a heat sink with fan for \$10 at the local computer store. I put it on top of the processor with some heat sink compound between, and anchored it in place at the corners with a little hot glue dribbled from corners to circuit board. I discovered that the hot glue didn't bond very well to the board and later added some clear silicone to hold the assembly together. I might explain that the heat sink was intended for a 486DX and thus didn't just clip in place. I noted and appreciated the speed increase of 4/3.

The best data transfer rate I saw on the 68000 system was about 90 Kbytes per second from its MFM hard drive. My present system hits 1,250,000 bytes per second. Loading an editor or a compiler is VERY fast. Now the computer does something and waits for its next instruction from me rather than the other way around.

Though the new computers are great and I wouldn't trade mine for something slower when I use it for program development or word processing using Windows TruType fonts and printing in graphics mode, there are numerous reasons why I would rather play with the old 6809 or 68000 system when I don't need the speed. The biggest reason is the simplicity of the old computers (and the software that runs on them). I have found that I can run versions of that old software on the new machine and it runs like lightning. For example my screen editor that I wrote years ago for the 6809 system is now running in a new and improved version (translated from PL/9 to C) with more features on the PC. WordStar for Windows takes a full minute to fire up. It must for some reason completely obscure to me, have to read 100 disk files before it can run. My old PAT editor loads as fast as I can type the command and get my finger on and off of the ENTER key. The .exe file is right around 50K of code. I suspect with Windows and WordStar running, I am using most of the 4 megs of RAM I have on the PC system.

You've seen over the past several issues how programming in Assembler is done. It looks (and is) rather easy for a small program, say a utility program. When programs get really large, one appreciates a faster computer. Our company has been using the 6809 for about 12 or 13 years now. We never found it inadequate to perform its intended purpose UNTIL our programs grew to the point that we were crowding the memory limit. Then it began to be a headache to try to squeeze code into the 48K or so that we could use for program code (We need some stack space and the I/O uses a bit of the memory address range).

Our reason for moving on was NOT the lack of capability of the small processor, but the lack of availability of sufficient memory for some of our larger applications. We began using multiple computers in some of our products, etc. The use of one of the new computers has given us a huge memory space, and a vast improvement in performance which we didn't know we needed until we had it. By that I mean that all the extra computing power has brought to mind things that we can do in our computer that we wouldn't have thought of earlier.

I guess the bottom line is pretty much the philosophy of The Computer Journal. If you need to do something complex use the latest 80X86 based 100 MHz computer. If you want to learn something about how computers work, go get an old microcomputer and dig in!

The TCJ Store

Regular Items

Back Issues S All Back Issues of TCJ are available.	ee page 44
TCJ Reference Cards\$3.00 So far, all we have is the Z80 Instruction Se Issue #77. These are on heavier stock than t with the issue.	t card from

The next two items are Group Purchase Items. TCJ doesn't have the resources to stock these for you, so we have to collect a minimum number of orders before we can provide these.

*GIDE kits\$73
Tilmann Reh's GIDE board was featured several is-
sues of TCJ. It is a 'Generic' IDE board to the Z80 that
plugs into the Z80 socket (you plug the Z80 back into the
GIDE board). This is still an experiment rs kit. Sample
code and docs including the articles from TCJ are pro-
vided, but you have to write you own BIOS routines.

Special Items

We currently have two each of Tilmann Reh's CPU280 boards and the IDE boards that go with them. The CPU280 was featured as the Centerfold in Issue #77 and the IDE interface was in Issue #56. These are bare boards and are not for the faint of heart. They are expensive and the parts are hard to get. But they're fast.

*CPU280 bare board	\$150
Comes with docs and utility disk.	
*IDE bare board	\$ 65
Comes with docs.	
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Kaenerbergstrasse 4
57076 Siegen (optional "-Weidenau")
GERMANY

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TCJ STAFF CONTACTS

- TCJ Editor: Dave Baldwin, (916)722-4970, FAX (916)722-7480 or TCJ BBS (916) 722-5799 (use "computer", "journal", pswd "subscriber" as log on), Email: tcj@psyber.com,.
- TCJ Adviser: Bill D. Kibler, PO Box 535, Lincoln, CA 95648, (916)645-1670, GEnie: B.Kibler, CompuServe: 71563,2243, E-mail: kibler@psyber.com.
- 32Bit Support: Rick Rodman, 1150 Kettle Pond Lane, Great Falls, VA 22066-1614. Real Computing BBS or Fax: +1-703-759-1169. E-mail: ricker@erols.com
- **Kaypro Support:** Charles Stafford, on the road somewhere. Email: CIS 73664,2470 (73664.2470@compuserve.com). TCJ has taken over Chuck's Kaypro parts and upgrade business.
- S-100 Support: Herb Johnson, 59 Main Blvd. Ewing, NJ 08618 (609)771-1503. Also sells used S-100 boards and systems. Email: hjohnson@pluto.njcc.com.
- 6800/6809 Support: Ronald Anderson, 3540 Sturbridge Ct., Ann Arbor, MI 48105.
- **Z-System Support:** Jay Sage,1435 Centre St. Newton Centre, MA 02159-2469, (617)965-3552, BBS: (617)965-7046; E-mail: Sage@ll.mit.edu.

REGULAR CONTRIBUTORS

- Brad Rodriguez, Box 77, McMaster Univ., 1280 Main St. West, Hamilton, ONT, L8S 1C0, Canada, E-mail: bj@headwaters.com..
- Frank Sergeant, 809 W. San Antonio St., San Marcos, TX 78666, E-mail: pygmy@pobox.com.
- Tilmann Reh, Germany, E-mail: tilmann.reh@hrz.unisiegen.d400.de. Has many programs for CP/M+ and is active with Z180/280 ECB bus/Modular/Embedded computers. Microcontrollers (8051).
- Helmut Jungkunz, Munich, Germany, ZNODE #51, 8N1, 300-14.4, +49.89.9614575. Email: helmut.jungkunz@metronet.de.

USER GROUPS

- Connecticut CP/M Users Group, contact Stephen Griswold, PO Box 74, Canton CT 06019-0074, BBS: (203)665-1100. Sponsors Z-fests.
- **SMUG**, Sacramento Microcomputer Users Group, has disbanded after all these years.
- CAPDUG: The Capital Area Public Domain Users Group, Newsletter \$20, Al Siegel Associates, Inc., PO Box 34667, Betherda MD 20827. BBS (301) 292-7955.
- NOVAOUG: The Northern Virginia Osborne Users Group, Newsletter \$12, Robert L. Crities, 7512 Fairwood Lane, Falls Church, VA 22046. Info (703) 534-1186, BBS use CAPDUG's.

- The Windsor Bulletin Board Users' Group: England, Contact Rodney Hannis, 34 Falmouth Road, Reading, RG2 8QR, or Mark Minting, 94 Undley Common, Lakenheath, Brandon, Suffolk, IP27 9BZ, Phone 0842-860469 (also sells NZCOM/Z3PLUS).
- NATGUG, the National TRS-80 Users Group, Roger Storrs, Oakfield Lodge, Ram Hill, Coalpit Heath, Bristol, BS17 2TY, UK. Tel: +44 (0)1454 772920.
- L.I.S.T.: Long Island Sinclair and Timex support group, contact Harvey Rait, 5 Peri Lane, Valley Stream, NY 11581.
- ADAM-Link User's Group, Salt Lake City, Utah, BBS: (801)484-5114. Supporting Coleco ADAM machines, with Newsletter/BBS.
- Adam International Media, Adam's House, 1829-1 County Road 130, Pearland, TX 77581-5040. Contact Terry Fowler for information. Web: "HTTP:// WWW.Flash.Net/~coleco"
- AUGER, Emerald Coast ADAM Users Group, PO Box 4934, Fort Walton Beach FL 32549-4934, (904)244-1516. Contact Norman J. Deere, treasurer and editor for pricing and newsletter information.
- MOAUG, Metro Orlando Adam Users Group, Contact James Poulin, 1146 Manatee Dr. Rockledge FL 32955, (407)631-0958.
- Metro Toronto Adam Group, Box 165, 260 Adelaide St. E., Toronto, ONT M5A 1N0, Canada, (416)424-1352.
- Omaha ADAM Users Club, Contact Norman R. Castro, 809 W. 33rd Ave. Bellevue NE 68005, (402)291-4405. Suppose to be oldest ADAM group.
- Vancouver Island Senior ADAMphiles, ADVISA newsletter by David Cobley, 17-885 Berwick Rd. Qualicum Beach, B.C., Canada V9K 1N7, (604)752-1984. dcobley@qb.island.net
- Northern Illiana ADAMS User's Group, 9389 Bay Colony Dr. #3E, Des Plaines IL 60016, (708)296-0675.
- San Diego OS-9 Users Group, Contact Warren Hrach (619)221-8246, BBS: (619)224-4878.
- The San Diego Computer Society (SDCS) is a broad spectrum organization that covers interests in diverse areas of software and hardware. It is an umbrella organization to various Special Interest Groups (SIGs). Voice information recordings are available at 619-549-3787.
- The Dina-SIG part of SDCS is primarily for Z-80 based computers from Altair to Zorba. The SIG sponsored BBS the Elephant's Graveyard (619-571-0402) is open to all callers who are interested in Z-80 and CP/M related machines and software. Contact Don Maslin, head of the Dina-SIG and the sysop of the BBS at 619-454-7392. Email: donm@cts.com.
- ACCESS, PO Box 1354, Sacramento, CA 95812, Contact Bob Drews (916)423-1573. Meets first Thurdays at SMUD 59Th St. (ed. bldg.).

- Forth Interest Group, PO Box 2154, Oakland CA 94621 510-89-FORTH. International support of the Forth language, local chapters.
- The Pacific Northwest Heath Users Group, contact Jim Moore, 1554 16th Avenue East, Seattle, WA 98112-2807. Email: be483@scn.org.
- The SNO-KING Kaypro User Group, contact Donald Anderson, 13227 2nd Ave South, Burien, WA 98168-2637.
- SeaFOG (Seattle FOG User's Group, Formerly Osborne Users Group) PO Box 12214, Seattle, WA 98102-0214.

OTHER PUBLICATIONS

- The Z-Letter has ceased publication.
- The Analytical Engine, by the Computer History Association of California, 4159-C El Camino Way, Palo Alto, CA 94306-4010. Home page: http://www.chac.org/chac/ E-mail: engine@chac.org
- **Z-100 LifeLine**, Steven W. Vagts, 2409 Riddick Rd. Elizabeth City, NC 27909, (919)338-8302. Publication for Z-100 (an S-100 machine).
- The Staunch 8/89'er, Kirk L. Thompson editor, PO Box 548, West Branch IA 52358, (319)643-7136. \$15/yr(US) publication for H-8/89s.
- The SEBHC Journal, Leonard Geisler, 895 Starwick Dr., Ann Arbor MI 48105, (313)662-0750. Magazine of the Society of Eight-Bit Heath computerists, H-8 and H-89 support.
- Sanyo PC Hackers Newsletter, Victor R. Frank editor, 12450 Skyline Blvd. Woodside, CA 94062-4541, (415)851-7031. Support for orphaned Sanyo computers and software.
- the world of 68' micros, by FARNA Systems, PO Box 321, Warner Robins, GA 31099-0321. E-mail: dsrtfox@delphi.com. New magazine for support of old CoCo's and other 68xx(x) systems.
- Amstrad PCW SIG, newsletter by Al Warsh, 6889 Crest Avenue, Riverside, CA 92503-1162. \$9 for 6 bi-monthly newsletters on Amstrad CP/M machines.
- Historically Brewed, A publication of the Historical Computer Society. Bimonthly at \$18 a year. HCS, 2962 Park Street #1, Jacksonville, FL 32205. Editor David Greelish. Computer History and more.
- IQLR (International QL Report), contact Bob Dyl, 15 Kilburn Ct. Newport, RI 02840. Subscription is \$20 per year. Email:IQLR@nccnet.com.
- QL Hacker's Journal (QHJ), Timothy Swenson, 5615 Botkins Rd., Huber Heights, OH 45424, (513) 233-2178, sent mail & E-mail, swensotc@ss2.sews.wpafb.af.mil. Free to programmers of QL's.
- Update Magazine, PO Box 1095, Peru, IN 46970, Subs \$18 per year, supports Sinclair, Timex, and Cambridge computers. Emil: fdavis@holli.com.

SUPPORT BUSINESSES

Hal Bower writes, sells, and supports B/PBios for Ampro, SB180, and YASBEC. \$69.95. Hal Bower, 7914 Redglobe Ct., Severn MD 21144-1048, (410)551-5922.

- Sydex, PO Box 5700, Eugene OR 97405, (541)683-6033. Sells several CP/M programs for use with PC Clones ('22Disk' format/copies CP/M disks using PC files system).
- Elliam Associates, PO Box 2664, Atascadero CA 93423, (805)466-8440. Sells CP/M user group disks and Amstrad PCW products. Email:??
- Discus Distribution Services, Inc. sells CP/M for \$150, CBASIC \$600, Fortran-77 \$350, Pascal/MT+ \$600. 8020 San Miguel Canyon Rd., Salinas CA 93907, (408)663-6966.
- Microcomputer Mail-Order Library of books, manuals, and periodicals in general and H/Zenith in particular. Borrow items for small fees. Contact Lee Hart, 4209 France Ave. North, Robbinsdale MN 55422, (612)533-3226.
- Star-K Software Systems Corp. PO Box 209, Mt. Kisco, NY 10549, (914)241-0287, BBS: (914)241-3307. SK*DOS 6809/68000 operating system and software. Some educational products, call for catalog.
- Peripheral Technology, 1250 E. Piedmont Rd., Marietta, GA 30067, (404)973-2156. 6809/68000 single board system. 68K ISA bus compatible system.
- Hazelwood Computers, RR#1, Box 36, Hwy 94@Bluffton, Rhineland, MO 65069, (314)236-4372. Some SS-50 6809 boards and new 68000 systems.
- AAA Chicago Computers, Jerry Koppel, (708)681-3782. SS-50 6809 boards and systems. Very limited quanity, call for information
- MicroSolutions Computer Products, 132 W. Lincoln Hwy, DeKalb, IL 60115, (815)756-3411. UNIFORM Format-translation, CompatiCard and UniDos products have been discontinued. Web page: http://www.micro-solutions.com.
- **GIMIX/OS-9**, GMX, 3223 Arnold Lane, Northbrook, IL 60062, (800)559-0909, (708)559-0909, FAX (708)559-0942. Repair and support of new and old 6800/6809/68K/SS-50 systems.
- n/SYSTEMS, Terry Hazen, 21460 Bear Creek Rd, Los Gatos CA 95030-9429, (408)354-7188, sells and supports the MDISK add-on RAM disk for the Ampro LB. PCB \$29, assembled PCB \$129, includes driver software, manual.
- Corvatek, 561 N.W. Van Buren St. Corvallis OR 97330, (503)752-4833. PC style to serial keyboard adapter for Xerox, Kaypros, Franklin, Apples, \$129. Other models supported.
- Morgan, Thielmann & Associates services NON-PC compatible computers including CP/M as well as clones. Call Jerry Davis for more information (408) 972-1965.
- Jim S. Thale Jr., 1150 Somerset Ave., Deerfield IL 60015-2944, (708)948-5731. Sells I/O board for YASBEC. Adds HD drives, 2 serial, 2 parallel ports. Partial kit \$150, complete kit \$210.
- Trio Company of Cheektowaga, Ltd., PO Box 594, Cheektowaga NY 14225, (716)892-9630. Sells CP/M (& PC) packages: InfoStar 1.5 (\$160); SuperSort 1.6 (\$130), and WordStar 4.0 (\$130).
- Parts is Parts, Mike Zinkow, 137 Barkley Ave., Clifton NJ 07011-3244, (201)340-7333. Supports Zenith Z-100 with parts and service.
- **DYNACOMP**, 178 Phillips Rd. Webster, NY 14580, (800)828-6772. Supplying versions of CP/M, TRS80, Apple, CoCo, Atari, PC/XT, software for older 8/16 bit systems. Call for older catalog.

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Regular Feature Editorial Comment Going Hi-Tech

The Computer Corner

By Bill Kibler

Welcome back to TCJ! I say that only because time is moving on and each issue is now taking some time to happen. Dave would love to move things faster than he is, but the rate of money coming into TCJ is rather slow. When I was editor, I would just dig deep into my pocket and find an extra thousand or so and keep on moving. Of course I never did get that money back and had to drop out as editor because of it. Dave however has no pockets to pull from and thus must print when he finally has the money.

I would love to help out and have a few times, but my own expenses have grown and I must make up for three years of losses. That of course explains why I am working on UNIX systems and doing C. I have almost recovered from the loss of sleep, free time, and money, only to look back and wish I could have made it work. Our time as the magazine supporting collectors is still around the corner, but systems like NT have people considering the old alternatives.

WINNT

Needing to pay for food and such has caused me to do regular programming on UNIX platforms. We use Win95 and WinNT platforms to run our tools on. These tools enable us to talk to the HP-Unix platforms and do our programming tasks. It gives me a chance to compare and understand better the advantages of simple and complex systems.

To show how much I have been converted to Unix, my fingers now work very automatically to move the cursor around in VI, the Unix editor. Vi is a little simple but very straight forward editor. On almost all platforms every

Unix programmer or administrator must know how to use it. Some even love it, I am not there yet. It is however some of these little Unix tools that can give you a good feeling about using that platform. The tools usually work (hear that M/S), a manual is online, and when you usually have a problem, someone has already created a tools for you. It also explains why so many Unix tools are ending up on PC's.

Now I have moved my own box at work from NT3.51 to NT4.0. I liked 3.51 better, mostly for it's regular windows setup (like 3.1). The new win95 desktop I find a drag, especially all the layers one must go through to change something. That of course depends on if you are allowed to change them at all. They have changed many tool names, removed some, replaced others. I have tried to add a parallel port hard drive to the box several times now, all without success. It says it is there, works, is running, but I am unable to get a drive letter.

Now under DOS I use the fdisk program to find out if I had a drive that was not setup correctly and thus was the reason it wasn't being seen. Fdisk is no where to be found in NT, nor can I find a way to test for an unformatted hard drive. It may be there, they just don't want you to find it without having gone to one of their special thousand dollar schools.

At this point I say give me Linux or plain old DOS, even CP/M would be better than this nonsense. But I have one item to top even this mess.

MMX

Well Intel has their new CPU (the

MMX or Pentium Pro, which is more Media Hype than horsepower upgrade) out and got one in the wings as well. I was reading an article in EETimes that caught my eye about the new CPU's. The units have power management built in, not to mention millions of transistors. This means they can idle back and save power when possible. These units also are run on anywhere from 1.8 to 3.5 volts depending on CPU speed, current needs, and tested performance at a given voltage. To do that a 4 or 5 bit signal is supplied to tell the power supply what voltage to select.

Two things came to mind, one the added complexity and a problem talked about in the article. I felt the complex-

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1	0	0	0	l
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1	0	0	1	1
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1	1	0	0	1
1	1	0	1	0
1	1	0	1	1
1	1	1	0	0
1	1	1	0	1
1	1	1	1	0
1 0	1 0	1 0	1 0	0
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0	0	0	0	0
0	0 0	0	0	0
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*note D4 all ones for backward compatiblity with older cpu types.

ity is partly to enable a better yield on the parts, as some chips were being chucked that fell outside some of the design parameters. However if the voltage is kept a bit low or hi these once rejected chips will now work just fine, or at least they think so. I am not sure it's worth the extra hassles and possible component costs and failures.

Those cost and problems were of course the main concern. You see the part can drop current usage to around 300 mills. But hit a key and zap your up to 12 Amps, yup 12 AMPS! That is a big change for any power supply, not to mention a whole lot of amps for a single CPU chip. I am not sure what gets me more, the switching from nothing to full power, or the fact that full power is 12 amps. You need some pretty big traces to handle those amps. not to mention the BIG spike such a current change will cause elsewhere in the system. Talk about a few design nightmares.

The Real World

Reading about all these changes makes me feel good about some of my other projects. I am still doing some 68HC11 work on the side. It is mostly C and moving along rather smoothly. I got a good laugh out of an article in a C support magazine. The writer was talking about doing embedded C++ and how a reduced set was needed. The funny part was how he started the article. He mentioned how most embedded products are too limited for C and especially C++.

This of course didn't stop him from continuing on talking about using C++ for embedded work. It is true a few organizations are using C and C++ for embedded systems, it is just those embedded products are very expensive and usually have DOD stamped all over them. I still have problems with people who use the same term for million dollar projects and those in which the whole product will cost less then ten dollars. We need a new list of terms so people can understand there is a big difference between these two extremes of the concept.

To me embedded systems generally have a cost of well under \$100 and are not a major design concern or cost.

Industrial real time control systems on the other hand are typically a major part of the cost. Maybe another idea is one that Dave keeps using, it's embedded if one person can do the design work, while it is an industrial controller if it takes a full staff to design and support the product. What terms might you think are best to separate these two very different fields of work. Send me an e-mail and I will list the ideas next time.

Product Failure

For those who wonder what has happened with our own CDROM project, I can say it is moving along slowly. I now have up and running a CCS and a GodBout S-100 system with 8 inch disks. Between the two I hope to start going back through all my old disks and some recently acquired disks looking for items of interests. My main interest is source to BIOS and utilities. So far I have a good collection, but few have been moved to my hard drive for cataloging.

Over the years I have heard many stories about users turning on their old systems only to get nothing. Well it finally happened to me the other day. I hadn't used several units in about three or four months and moved them into position to help with the disk cataloging. I tried three of the Z100's that had worked earlier and one was still connected to the 8 inch drives I was also going to use for copying. Well you can probably guess that not a one of the units would boot up. A couple had video problems, one just wouldn't boot no matter what. I finally gave up for now and dug out an older terminal and used that to test the S-100 systems with.

My idea had been to use a Z-100 for a terminal with the occasional copy when one of the S-100 systems wouldn't read the 8" disk. The Z-100 also can copy from CP/M disk to MSDOS disk using one of their own utilities. Later checking showed the problem to be water damage that eaten away some of the traces and messed up one of the sockets. Where the water came from, I have no idea, but what a mess. I now have a better understanding of the frustration so many of you have told me about. However don't

think using PC's will keep it from happening.

I got a panic call from an old friend who has some knowledge of computers. His major skill set is two-way radio which he did till he retired recently. He has played with computers some, but does not yet have the full grasp of what can go wrong. I have tried to help him resolve problems with windows which only frustrated him more as we often hit one wall or another.

This problem had to do with adding a second printer, in this case one of the newer Epson. When attempting to send data to it, he got back a paper out message, no matter what. My friend had gotten a second parallel port card for his PC. When trying that card, nothing work, and thus a phone call to me. I re-checked all he did and drug the printer home where it tested just fine.

I went back the next day and tried a few more things. First I checked the new parallel card and decided all the jumpers needed to be opposite from what the tech at the store told him. I used MSD and had a different, or OK status report on the two printer ports. Now that we knew the PC tech was wrong and one problems was conflicting port addresses, we tried the printers again.

After a few minor tests, all started to work properly. The problem it seems starts with his old parallel port which gives a paper out error on the Epson no matter what, a mis-configured second board, and not enough experience to know that most computer store techs have trouble using the correct end of a screwdriver. I guess at this point I need to do my normal complaint and say how bad it is and all, but I did that far too many times already, so I will just let it pass.

Till Next Time

Speaking of passing, I just ran out of space, so hope your trials and tribulations are minor ones, and keep hacking. Bill.

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